On-Wafer Calibration Techniques Enabling Accurate Characterization of High-Performance Silicon Devices at the mm-Wave Range and Beyond

Von der Fakultät für Maschinenbau, Elektrotechnik und Wirtschaftsingenieurwesen der Brandenburgischen Technischen Universität Cottbus-Senftenberg zur Erlangung des akademischen Grades eines Doktors der Ingenieurwissenschaften (Dr.-Ing.) genehmigte Dissertation

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1 MOTIVATION

1.1 Advances in Silicon Technologies for mm-Wave Applications

The continuously increasing demand for more content, services, and security drives the development of high-speed wireless technologies, optical communication, automotive radar, imaging and sensing systems and many other mm-wave and THz applications. Commercialization, the need for highly-integrated and cost-effective circuits and systems push the transition of mm-wave and sub mm-wave devices and circuits from III-V materials to silicon that is more attractive for consumer market (e.g., [1]).

As Harame stated in [2], both the Complementary Metal Oxide Semiconductor (CMOS) and the Bipolar CMOS (BiCMOS) technologies play an important role in the commercial RF and mm-wave applications. While the BiCMOS is favored for high performance applications with low digital content, the price advantage for the high-volume production stimulates the further optimization of the RF CMOS for the needs of mm-wave applications (Fig. 1.1).

Due to shrinking lateral device geometries and technology improvement it became possible to achieve operation frequencies of half of THz for silicon-germanium SiGe:C Heterojunction Bipolar Transistors (HBTs) [3]. Several ongoing European projects aimed to realize SiGe HBTs operating at a maximum frequency up to 0.7 THz, as well as to integrate and to optimize back-end modules in an advanced 55 nm technology. This would enable a 0.5 THz 55 nm SiGe BiCMOS platform for design of RF, mm-wave and THz system-on-chip for commercial applications [4, 5].

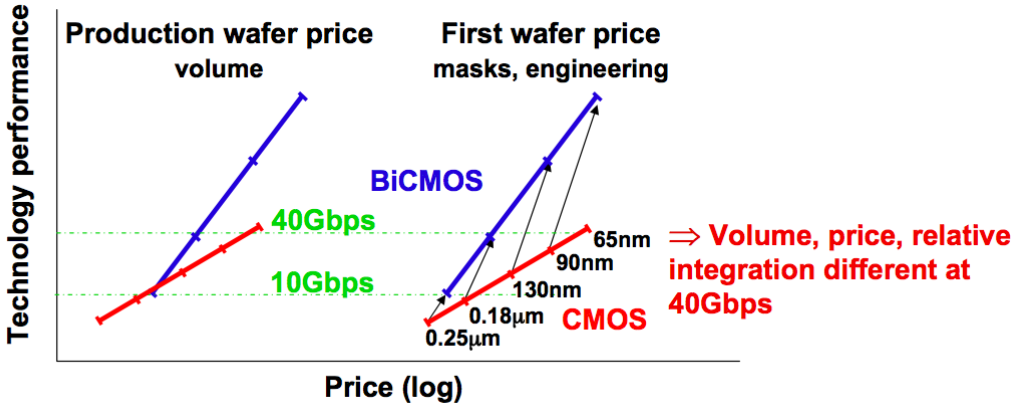


Fig. 1.1: Performance vs. price for silicon technology generations. Picture from [6].

1.2 Challenges of RF Characterization of Advanced Devices

S-parameter measurement at mm-wave and sub-mm wave frequencies plays a crucial role in the IC design debug. Most important, however, is the step of device characterization for development and optimization of device model parameters for new technologies. Accurate characterization of the intrinsic device in its entire operation frequency range becomes extremely important. It enables truthful extraction of the device model parameters radically decreasing IC design iterations and, as a result, the development time and cost. Thus, the need for accurate, reliable, and easy for implementation procedures for intrinsic device characterization at mm-wave frequencies and beyond drastically increases.

Calibrating of S-parameter measurement system is crucial already at relatively low frequencies of hundreds of megahertz: the wavelength of the test signal is of several orders of magnitude shorter than the equivalent length of the measurement signal path. The RF calibration is intended to remove systematic errors from the instrument hardware (and to take into account the presence of any accessories that may have been added to enable specific measurements to be performed) at the required frequencies for the measurements. For example, measurements may be required to be made in an on-wafer environment. In this case, first cables need to be connected to the measurement instrument (Vector Network Analyzer, or VNA) front panel connectors, followed by coaxial adaptors, and finally on-wafer probes. RF calibration will correct for the impact of these added components as well correct the systematic errors in the instrument. This is why this type of calibration is often referred to as “error correction” (Fig. 1.2).

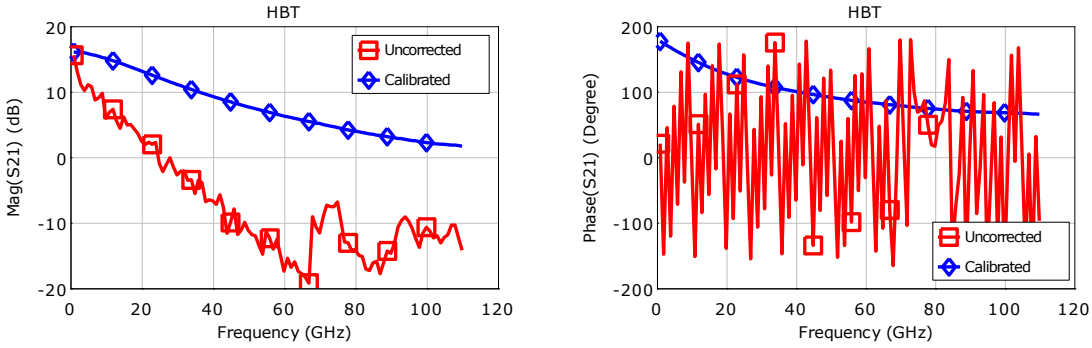


Fig. 1.2: Uncorrected and calibrated measurements of gain of the same transistor.

The error correction procedure can also be imagined as a virtual shifting of the measurement reference plane (i.e. the “zero point” of the magnitude and phase of the measurement signal) to desired location. For example, the calibration procedure sets the measurement reference plane to the cable end for measurements in coaxial environment. The systematic measurement errors are defined using the set of coaxial

calibration standards – the calibration kit. Conventionally, the characterization of the RF devices at the wafer level is done with the respect to the probe-tip calibration. In this case, the measurement reference plane is set close to the end of the RF probes using planar calibration standards.

Vendors of RF probes provide probe-tip calibration standards and verification elements and guarantee accurate system calibration and calibration accuracy verification at the wafer-level. A simple short-open-load-thru (SOLT) method that is available from the front panel of every VNA can successfully be used with the probe-tip standards at frequencies up to 20 GHz at least [7]. Thus, calibration of the measurement system, the calibration validation as well as the sharing of the measurement data between different parties is relatively simple and is well-established.

The RF probe-tip calibration provides the appropriate error correction for measurement of integrated circuits (ICs). The characterizing of an intrinsic device, however, is associated with additional challenges: the parasitic impedance of the device contact pads, interconnect lines and via stack is of some order of magnitude greater than the input and output impedances of the device itself. The contact pad de-embedding procedure is a conventional solution of this problem. Usually, two special elements, so-called de-embedding open and short dummies, are placed on the wafer close to the DUT. They are laid out so that they represent the parallel and the serial portion of the device parasitic impedances. Therefore, both parasitic components can be measured together with the DUT and then subtracted from the DUT measurement results in two steps: first its parallel portion followed by the serial portion. With other words, the pad de-embedding shifts the measurement reference plane from the probe tip further towards the device terminals.

The accuracy of the two-step de-embedding decreases with the frequency and becomes unsatisfactory above already 40 GHz. As many publications already showed, the approximation of the device parasitic impedance over just two parallel and serial equivalent components is insufficient at mm-wave frequencies. The parasitic impedance becomes of more complex nature; the portion of its distributed component drastically increases. Though several advanced de-embedding methods already demonstrated reasonable accuracy improvement at mm-wave frequencies, they did not find a wide application on practice. Utilizing complex approaches for more accurate capturing of the Backend of Line (BEOL) parasitics, they require five, six or more dummy elements, measurement and post-processing steps. It significantly increases the complexity of the method, the difficulty of its practical implementation. The risk of errors is also increased, often leading to such common mistakes as under- and/or over-de-embedding. That is why the device model parameters are extracted for the 40 GHz (often even 20 GHz) measured and de-embedding using the two-step method, as International Technology Roadmap for Semiconductors (ITRS) describes in [8]. Such compromise is justified by two factors:

1. It is a common understanding that the compact model parameters of a device such as, for instance, its junction capacitances should be constant over the wide frequency range;
2. The simplicity of the de-embedding step.

However, the extraction of another important device (and technology) Figure of Merits (FoM) suffer from this compromise: the unity current gain cut-off frequency f_T and the unity power gain (the maximum oscillation frequency) f_{MAX} (Fig. 1.3). Both parameters are depended on the device geometry and are extremely sensitive to the device parasitics. Because the solution for accurate characterization of the intrinsic device up to sub-THz frequencies (this is the range of performance of the modern advanced devices) is not yet available, f_T and f_{MAX} are extrapolated from the data that are obtained much below 110 GHz.

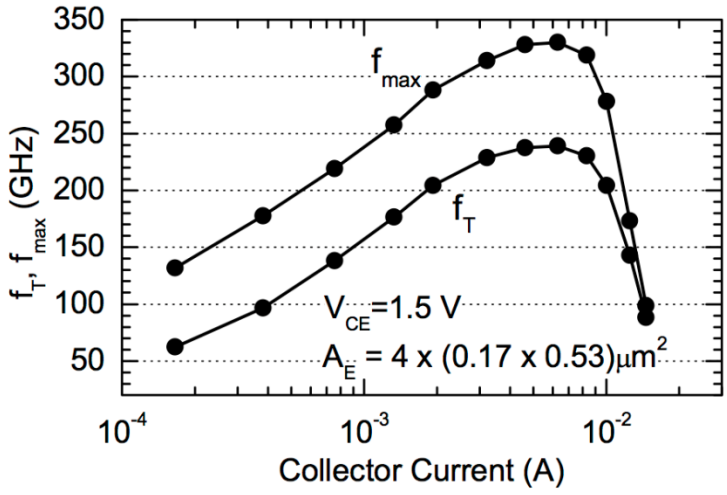


Fig. 1.3: f_T and f_{MAX} of a high-speed SiGe BiCMOS HBT as a function of collector current extrapolated from h_{21} and the unilateral gain U at 40 GHz. Picture from [9].

It is still a subject of hard debates within the modeling engineer community which method of the extraction of f_T and f_{MAX} provides reliable results (e.g. [8, 10-13]). Different methods may show up to 30% variation of the extrapolated parameters. With any further progress step in the device performance, it becomes more difficult to justify the sub-THz values of f_{MAX} that are extracted from data measured below 65 GHz (e.g. [14, 15]). A good example of such situation is shown on the Fig. 1.4. The values of the $f_T = 521$ GHz $f_{MAX} = 1.15$ THz were extracted from 50 GHz data. Measurement results of the same device at frequencies from 75 GHz to 110 GHz are less accurate and may lead to very different extraction results. Obviously, the need for accurate characterization of the intrinsic device at mm-wave and sub-mm-wave frequencies turned out to be more meaningful and critical for advanced technologies featuring sub-THz f_T and f_{MAX}.

Advanced mm-wave and sub-mm-wave III-Vs semiconductor technologies (e.g. Gallium Arsenide GaAs, Gallium Nitride GaN, and Indium Phosphide InP) do not utilize multiple metallization layers, typically only two (e.g. [16]). Technology steps mostly address vertical and horizontal scaling of a lateral device (e.g. [17]). That is why the measurement reference plane can be shifted from the probe tip close to intrinsic device terminals by either a simple two-step de-embedding or straightforward by implementing the *in-situ* calibration (e.g. [14, 18]).

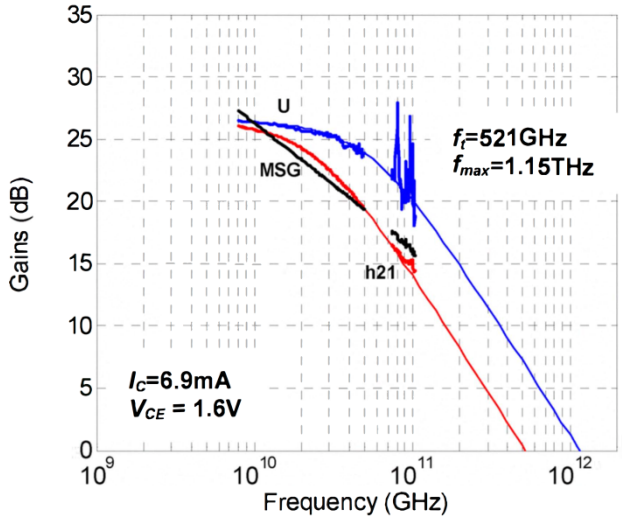


Fig. 1.4: Extrapolated f_T and f_{MAX} of a 0.13 µm x 2µm HBT from the 130 nm InP process. The device is measurement up to 50 GHz and from 75 GHz to 110 GHz. Picture from [14].

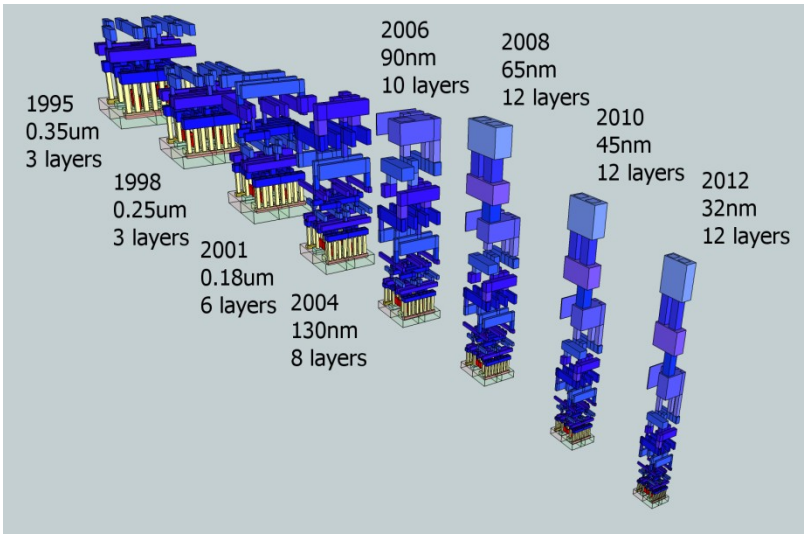


Fig. 1.5: An inverter realized in different silicon technologies: from the 0.35 um to the 32 nm CMOS processes. The device layout is simulated based on the ITRS data. Picture is courtesy of Akira Tsuchiya (Kyoto University, Japan).

A progress of the silicon technologies is more complex. Fig. 1.5 shows the same simple inverter as being realized from the 0.35 um to 32 nm CMOS processes according to the ITRS data. Together with the downscaling if a lateral device, every next step of the silicon technologies adds more metal layers to the process BEOL. As a result, the extraction of reliable FoM using conventional methods becomes more and more challenging: the device performance level increase, its parasitic resistances and capacitances are reduced and the BEOL parasitics are drastically increased. The need for the new calibration methods that can sufficiently improve the characterization accuracy

of the intrinsic device and, at the same time will be simple for practical implementation is drastically increasing.

1.3 Contribution of This Work

This work addressed the change of accurate mm-wave characterization of devices fabricated in advanced semiconductor technologies. It developed the *in-situ* calibration solution that is easy to be implemented for silicon technologies. The new technique was verified up to 110 GHz on three difference processes: high performance SiGe:C BiCMOS from IHP Microelectronics (Germany), BiCMOS9MMW from STMicroelectronics (France), and RF CMOS 8SF from IBM Microelectronics (USA). Practical results demonstrated that proposed *in-situ* calibration significantly outperforms the convention method independently on the process specifics and complexity.

In this work, several RF calibration methods were analyzed and it was shown that two of them were good candidates for the *in-situ* application: the multiline TRL[1] and the transfer TMR[2]. The accuracy of both methods was verified qualitatively and quantitatively. While the experimental data proved that that both methods are comparable to each other from the measurement accuracy perspective, the multiline TRL was recommended for the technology development step while the transfer TMR was suggested for the final production step. It was also shown how this *in-situ* calibration solution can be expanded to address the needs of multiport measurements.

A special attention was given to such topics as:

1. Specifics of wafer-level measurement and calibration caused by application of planar calibration elements as well as advantages and drawbacks of S-parameter calibration methods for the *in-situ* system calibration;
2. The optimal location of the *in-situ* calibration reference plane. The proposed solution addressed the needs of device modeling engineers, circuit designers and the characterization engineers, as well as the specific requirements rising at sub-mm-wave frequencies;
3. Design rules for the on-wafer calibration standards. The developed design recipe can be successfully applied for CMOS and BiCMOS silicon processed as well as on III-Vs semiconductors;
4. Definition of electrical properties of custom standards. Detailed analysis and the extensive number of experiments yielded to a list of simple recommendations for specifics of every calibration method. The variation of the standard properties caused by the instability of the fabrication process and the need for measurements at multiple temperatures was also addressed;
5. Verification of the calibration accuracy. The work presented results of the quantitative verification of the *in-situ* calibration accuracy using the method

[1] Thru-Reflect-Line
[2] Thru-Match-Reflect

proposed by the National Institute of Standards and Technology (NIST, USA). It also proposed a simple qualitative verification method that is simple for practical applications.

Some important aspects of the on-wafer S-parameter measurement assurance were presented as well. The discussion included the analysis of the calibration residual errors caused by the improper boundary conditions of coplanar calibration standards and the impact of the RF probe tip design. In conclusion, some suggestions for further accuracy improvement of the proposed method are given.

2 INTRODUCTION

2.1 S-Parameters of a Linear Network

Electrical behavior of a linear n-port device is usually described over its input and output impedance or admittance parameters (Z- or Y-parameters respectively). These parameters are defined as voltage V and current I relationship at input and output ports of the device connected to a generator and terminated to an open or a short circuit (Fig. 2.1). With increase of operation frequency, the realization of an ideal open or short termination becomes more challenging. Moreover, many types of DUTs (*e.g.* filters, power amplifiers) cannot be measured in this way as shortcutting their output can change the electrical characteristics or even destroy the device. Instead, another set of parameters is commonly used to describe a behavior at high frequencies: the *scattering*, or S-parameters. S-parameters define the relation between the incident, reflected and transmitted power waves at each device terminal under specified load conditions. S-parameters are significantly easier to be measured. If required, they can be converted to other parameters, such as Z, Y, T, H (e.g. [19]).

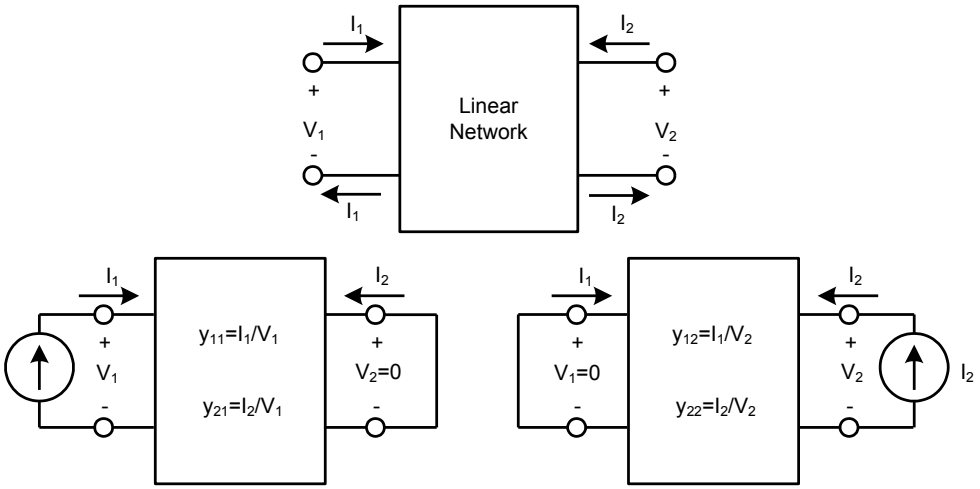


Fig. 2.1: A linear network (top) and definition of its Y-parameters (bottom).

In [20], Kurokawa proposed a concept of incident a and reflected b power waves that simplified the analysis of microwave networks:

$$a_i = \frac{V_i + Z_i I_i}{2\sqrt{|\Re(Z_i)|}}, \tag{2.1}$$

$$b_i = \frac{V_i - Z_i^* I_i}{2\sqrt{|\Re(Z_i)|}}, \tag{2.2}$$

where V_i and I_i are voltage and current flowing into the ith port of a junction. Z_i is the impedance of the ith port. Z_i^* is the complex conjugate of Z_i.

The ratio of a_i and b_i gives the power wave reflection coefficient:

$$s = \frac{b_i}{a_i}. \tag{2.3}$$

For a linear n-port network with vectors a, b, v and i the ith components are a_i, b_i, V_i and I_i at its ith port. So, a and b can be written in terms of v and i as:

$$a = F(v + G_i),\, b = F(v - G^+ i), \tag{2.4}$$

where F and G are the diagonal matrices. Their ith diagonal components are $1/2\sqrt{|\Re Z_i|}$ and Z_i, respectively. G^+ is the complex conjugate transposed matrix of G.

The linear relationship between v and i as well as b and a are given by:

$$v = Z \cdot i \text{ and } b = S \cdot a, \tag{2.5}$$

where Z is the impedance matrix and S is the power wave scattering matrix.

The i, jth element of the scattering matrix is:

$$S_{ij} = \frac{b_i}{a_j}\bigg| a_k = 0,\ k \neq j. \tag{2.6}$$

An example for a two-port network is shown in Fig. 2.2. S_{11} and S_{22} are its forward and reverse reflection parameters, while S_{21} is the transmission parameter for forward (from port 1 to port 2) and S_{12} for reverse (from port 2 to port 1) directions respectively. Often, S-parameters of a network are presented as a flow graph (Fig. 2.2, right).

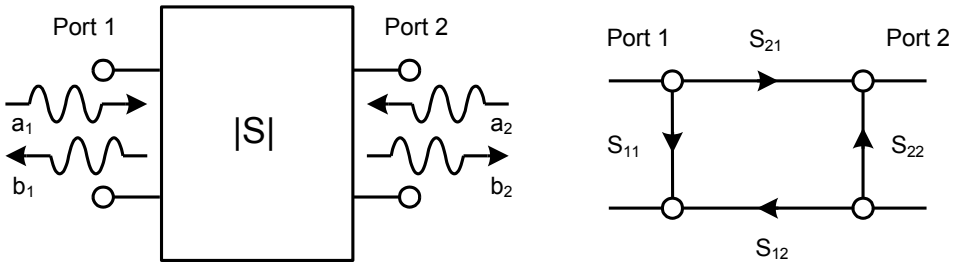


Fig. 2.2: Definition of incident and reflected waves (left) and the signal flow graph of a two-port network (right).

2.2 Theory of a Uniform Waveguide Mode

Marks and Williams introduced in [21] an alternative set of parameters, the “pseudo waves”, that are more applicable for developing VNA calibration techniques at the wafer level. At the wafer-level, the measurement reference impedance Z_{REF} and the characteristic impedance of the transmission media Z_0 often do not equal each other.

This section, gives a short compendium from the Marks’ and Williams’ General Waveguide Circuit Theory. It is essential for this work and it will be regularly referred to from other sections.

2.2.1 Waveguide Voltage and Current

For given the waveguide voltage v and the waveguide current i, the transverse components of the total electrical and magnetic fields $\boldsymbol{E}$ and $\boldsymbol{H}$ can be represented by:

$$\mathbf{E}_t = c_+ e^{-\gamma z}\mathbf{e}_t + c_- e^{+\gamma z}\mathbf{e}_t \equiv \frac{v(z)}{v_0}\cdot\mathbf{e_t}, \tag{2.7}$$

$$\mathbf{H}_t = c_+ e^{-\gamma z}\mathbf{h}_t + c_- e^{+\gamma z}\mathbf{h}_t \equiv \frac{i(z)}{i_0}\cdot\mathbf{h_t}, \tag{2.8}$$

where:

$\boldsymbol{e_t}$ and $\boldsymbol{h_t}$ are the transverse components of the electric and magnetic fields, respectively;

γ is the propagation constant composed of real α and imaginary β components as: $\gamma \equiv \alpha + j\beta$;

z is the longitudinal unit vector;

v_0 and i_0 are the normalization constants, so both v and v_0 have units of voltage and i and i_0 have units of current.

The fields $\boldsymbol{e}_t$ and $\boldsymbol{h}_t$ are in the normalized forward-propagating mode with the propagation constant γ, waveguide voltage $v(z) = v_0 e^{-\gamma z}$, and waveguide current $i(z) = i_0 e^{-\gamma z}$. For the normalized backward-propagating mode, the propagation constant is $-\gamma$, $u(z) = v_0 e^{+\gamma z}$, and $i(z) = -i_0 e^{+\gamma z}$.

2.2.2 Power

The net complex power $p(z)$ crossing a transverse plane S is given by:

$$p(z) \equiv \int_S \boldsymbol{E_t} \times \boldsymbol{H_t^*} z \mathrm{d}S = \frac{v(z) i^*(z)}{v_0 i_0^*} p_0, \tag{2.9}$$

where:

$$p_0 \equiv \int_S \boldsymbol{e_t} \times \boldsymbol{h_t^*} z \mathrm{d}S. \tag{2.10}$$

Imposing the constraint:

$$p_0 = v_0 i_0^*, \tag{2.11}$$

the condition

$$p = v i^* \tag{2.12}$$

can be achieved with arbitrary choices of the normalization constants v_0 and i_0. Equations (2.9) and (2.12) can be simultaneously satisfied. When choosing v_0 or i_0 arbitrary, the other will be defined by equation (2.11).

The average power flow $P(z)$ across the section S is given by the real part of $p(z)$ as:

$$P(z) \equiv \Re(p(z)) = \Re\left(\int_S \boldsymbol{E_t} \times \boldsymbol{H_t^*} z \mathrm{d}S \right) = \Re(v i^*). \tag{2.13}$$

This leads to the conclusion that the power is *not* generally a linear combination of the forward and backward mode powers, since it is given by a nonlinear expression. This means that the net real power P is in general *not* simply the difference of the power carried by the forward and backward modes.

2.2.3 Characteristic Impedance

The characteristic impedance Z_0 of the forward mode is defined by:

$$Z_0 = \frac{v_0}{i_0} = \frac{|v_0|^2}{p_0^*} = \frac{p_0}{|i_0|^2}. \tag{2.14}$$

Definition (2.14) is an analogy to the electrical circuit theory. It is important to note that Z_0 is independent from the normalization of the modal fields $\boldsymbol{e}$ and $\boldsymbol{h}$, which affect $|p_0|$. While the magnitude of Z_0 does depend on the choice of either v_0 or i_0, its phase is identical to that of p_0 and therefore independent of all normalizations. The phase of the characteristic impedance Z_0 is a fixed, inherent, and unambiguous property of the mode.

Marks and Williams give an example of the special case of TE (transverse electric), TM (transverse magnetic), or TEM (transverse electromagnetic) modes in homogeneous matter to illustrate the close correspondence between their definition of Z_0 and the conventional definition of the characteristic impedance. Assuming that the waveguide impedance η is constant over the cross section, each mode has fields that satisfy:

$$z \times \boldsymbol{e}_t = \eta \boldsymbol{h}_t. \tag{2.15}$$

So, Z_0 is given by:

$$Z_0 = \frac{|v_0|^2}{\int_S |\boldsymbol{e}_t|^2 \mathrm{d}S}\eta. \tag{2.16}$$

The last proves that the phase of the characteristic impedance is equal to that of the wave impedance: the modal field $\boldsymbol{e}_t$ is normalized, the denominator is fixed and the magnitude of Z_0 depends only on v_0.

2.2.4 Equivalent Circuit Representation of Transmission Line

The four parameters that are used to describe a section of a transmission line are capacitance C, inductance L, resistance R, and conductance G per unit length (Fig. 2.3):

$$j\omega C + G \equiv \frac{\gamma}{Z_0}, \tag{2.17}$$

$$j\omega L + R = \gamma Z_0. \tag{2.18}$$

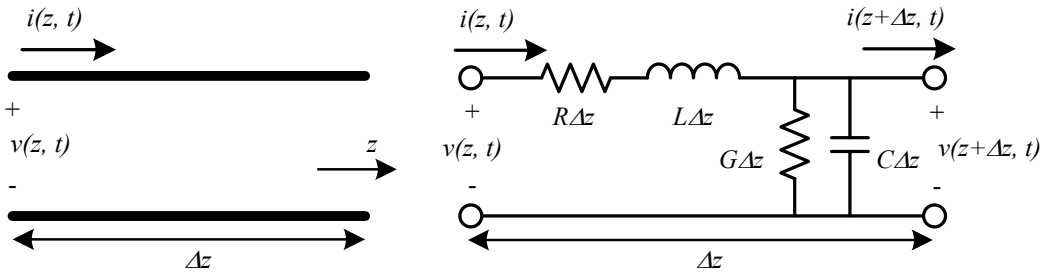


Fig. 2.3: The voltage and current definitions and the equivalent circuit of an incremental length of a transmission line.

Also, these parameters often appear in equations satisfied by v and i (e.g. [19]):

$$\frac{\mathrm{d}v}{\mathrm{d}z} = (j\omega L + R)i, \tag{2.19}$$

$$\frac{\mathrm{d}i}{\mathrm{d}z} = -(j\omega C + G)v. \tag{2.20}$$

From (2.17) and (2.18), the propagation constant γ and the characteristic impedance Z_0 of the line are defined as:

$$\gamma = \sqrt{(j\omega L + R)(j\omega C + G)}, \tag{2.21}$$

$$Z_0 = \sqrt{\frac{j\omega L + R}{j\omega C + G}}. \tag{2.22}$$

Both equations (2.21) and (2.22) have two roots corresponding to the forward and backward propagation modes. Each mode has identical C, L, G, and R but opposite γ and Z_0. For the forward mode, $\Re(Z_0) \geq 0$ and hence its γ can be calculated from either (2.17) or (2.18).

2.2.5 *Effective Permittivity and Measurement of Characteristic Impedance*

Effective permittivity $e_{r,eff}$ (also called effective relative dielectric constant) equates to the propagation constant γ of a TEM mode in a fictitious medium of permittivity $e_{r,eff}e_0$ and permeability μ_0. It is defined as:

$$e_{r,eff} \equiv -\left(\frac{c\gamma}{\omega}\right)^2, \tag{2.23}$$

where c is the speed of light in vacuum.

Using (2.21), we can define:

$$e_{r,eff} = \frac{c^2}{\omega^2}\left(\omega^2 LC - RG - j\omega(LG + RC)\right). \tag{2.24}$$

In most cases, C, L, G, and R are nonnegative, which leads to: $\Im(e_{r,eff}) \leq 0$. Typically, $\Re(e_{r,eff}) > 0$, however it becomes negative in lossy lines at low frequencies when $RG > \omega^2 LC$.

The equation (2.22) can be re-written as:

$$Z_0 = \frac{\sqrt{e_{r,eff}}}{c \cdot C\left(1 + \frac{G}{j\omega C}\right)}, \tag{2.25}$$

which can be applied for the determination of Z_0 [22]. This relation will be used further to measure characteristic impedance of commercial and custom line standards.

2.3 Waveguide Circuit Theory

These results were essential for the development of Marks' and Williams' waveguide circuit theory. This section will first show how they defined the travelling and the

pseudo-travelling waves for a single uniformed waveguide. Next, it will present the scattering and the pseudo-scattering parameters, impedance matrices and transformation of the reference impedance, as given in the General Waveguide Circuit Theory [21].

2.3.1 Travelling Wave

The forward and backward travelling waves a_0 and b_0 are derived by normalizing the forward and backward modes in (2.7) and (2.8):

$$a_0 \equiv \sqrt{\Re(p_0)}c_+e^{-\gamma z} = \frac{\sqrt{\Re(p_0)}}{2v_0}(v + iZ_0) \tag{2.26}$$

and

$$b_0 \equiv \sqrt{\Re(p_0)}c_-e^{+\gamma z} = \frac{\sqrt{\Re(p_0)}}{2v_0}(v - iZ_0) \tag{2.27}$$

for positive roots. Both a_0 and b_0 are independent of the magnitude of the modal field $\boldsymbol{e}_t$. The phases of a_0 and b_0 depend on the phase of $\boldsymbol{e}_t$ in the same way as the phases of c_+ and c_- do.

Assuming that $\Re(Z_0) \neq 0$, (2.26) and (2.27) can be re-written as:

$$v(z) = \frac{v_0}{\sqrt{\Re(p_0)}}(a_0 + b_0), \tag{2.28}$$

$$i(z) = \frac{i_0}{\sqrt{\Re(p_0)}}(a_0 - b_0). \tag{2.29}$$

Therefore, the real power results from (2.13):

$$P(z) = |a_0|^2 - |b_0|^2 + 2\Im(a_0 b_0^*)\frac{\Im(Z_0)}{\Re(Z_0)}. \tag{2.30}$$

Equation (2.30) demonstrates that the real net power P crossing a reference plane is not equal to the difference of the powers carried by the forward and the backward waves. The only exception is when the characteristic impedance is real or when either a_0 or b_0 vanish.

Reflection coefficient Γ_0 is defined by:

$$\Gamma_0(z) \equiv \frac{b_0(z)}{a_0(z)}. \tag{2.31}$$

The power can be expressed in terms of reflection coefficient as:

$$P = |a_0|^2 \left(1 - |\Gamma_0|^2 - 2\Im(\Gamma_0)\frac{\Im(Z_0)}{\Re(Z_0)}\right). \tag{2.32}$$

It is important to note that $|\Gamma_0|^2$ is not a power reflection coefficient and it may exceed 1 if Z_0 is not real.

2.3.2 Pseudo-Waves

For wafer-level measurements, it turned to be more suitable to introduce *pseudo-waves* as an alternative set of parameters. Pseudo-waves are the mathematical artifacts defined for a specific reference impedance Z_{ref} which satisfy $\Re(Z_{ref}) \geq 0$. The complex pseudo-wave amplitudes a and b are defined as:

$$a(Z_{ref}) \equiv \left(\frac{|v_0|}{v_0}\frac{\sqrt{\Re(Z_{ref})}}{2\,|Z_{ref}|}\right)(v + iZ_{ref}) \tag{2.33}$$

and

$$b(Z_{ref}) \equiv \left(\frac{|v_0|}{v_0}\frac{\sqrt{\Re(Z_{ref})}}{2\,|Z_{ref}|}\right)(v - iZ_{ref}). \tag{2.34}$$

Therefore, v and i can be described inversely as:

$$v = \left(\frac{v_0}{|v_0|}\frac{|Z_{ref}|}{\sqrt{\Re(Z_{ref})}}\right)(a + b) \tag{2.35}$$

and

$$i = \frac{1}{Z_{ref}}\left(\frac{v_0}{|v_0|}\frac{|Z_{ref}|}{\sqrt{\Re(Z_{ref})}}\right)(a - b). \tag{2.36}$$

The positive root must be chosen for (2.33) through (2.36). This leads to the re-definition of the average power from (2.13) as:

$$P = |a|^2 - |b|^2 + 2\Im(ab^*)\frac{\Im(Z_{ref})}{\Re(Z_{ref})}. \tag{2.37}$$

The pseudo-reflection coefficient Γ is defined by:

$$\Gamma(Z_{ref}) \equiv \frac{b(Z_{ref})}{a(Z_{ref})} \tag{2.38}$$

and depends on Z_{ref}. Finally, the power P can be expressed over the reflection coefficient (from (2.32)):

$$P = |a|^2 \left(1 - |\Gamma|^2 - 2\Im(\Gamma)\frac{\Im(Z_{ref})}{\Re(Z_{ref})}\right). \tag{2.39}$$

Obviously, the pseudo-waves are equal to the actual travelling waves when the reference impedance is set to be the characteristic impedance of the mode. However, this is not always convenient. So, in case of a lossy and dispersive planar transmission line, it makes more sense to use a constant reference impedance (such as $Z_{ref} = 50\ \Omega$), because the characteristic impedance varies significantly with the frequency [22, 23]. Thus, the measurement results for $Z_{ref} = Z_0$ may be difficult to interpret.

Another convenient choice is to set Z_{ref} such that $b(Z_{ref})$ vanishes at a given point on the line. Thus, the pseudo-reflection coefficient cancels out at a particular z and for a particular termination. Many calibration methods use this approach and force the pseudo-reflection coefficients of some calibration standards (typically "match" or "load") to vanish. A good example is the conventional LRM [24]. It is often used in coaxial measurement environment and is hardly applicable at the wafer level for planar standards. This problem was recognized already at early stages of the wafer-level RF measurement technology and facilitated the development of dedicated methods (e.g. [25]). A special attention to this problem is given later in this work (see Chapter 3 and Chapter 4).

2.3.3 Scattering and Pseudo-Scattering Matrices

For a linear waveguide circuit with a typical multiport configuration, one can define the reference impedance Z^i_{ref} at each waveguide port i with $a_i(Z^i_{ref})$ and $b_i(Z^i_{ref})$ given by (2.33) and (2.34). Similar to (2.5), the vector of the outgoing pseudo-waves $\mathbf{b}$ is linearly related to the vector of incoming pseudo-waves $\mathbf{a}$ by a pseudo-scattering matrix $\mathbf{S}$:

$$\mathbf{b} = \mathbf{S}\mathbf{a}. \tag{2.40}$$

Similarly, the scattering matrix $\mathbf{S^0}$ is defined as the relation of the vectors $\mathbf{a}_0$ and $\mathbf{b}_0$ (vectors of incoming a^i_0 and outgoing b^i_0 waves):

$$\mathbf{b}_0 = \mathbf{S^0}\mathbf{a}_0. \tag{2.41}$$

The pseudo-scattering matrix $\mathbf{S}$ is equal to the scattering parameter matrix $\mathbf{S^0}$ if $Z^i_{ref} = Z^i_0$ at each ith port.

For a one-port, the reflection coefficients Γ_0 and Γ are the single elements of scattering matrices $\mathbf{S}_0$ and $\mathbf{S}$.

2.3.4 The Cascade Matrix

Often, it is more practical to operate with so called transmission "T" or cascade parameters. Similar to (2.40), the pseudo-cascade parameter matrix is given as:

$$\begin{bmatrix} b_1(Z_{ref}^i) \\ a_1(Z_{ref}^i) \end{bmatrix} = T^{ij} \begin{bmatrix} a_2(Z_{ref}^i) \\ b_2(Z_{ref}^i) \end{bmatrix}, \tag{2.42}$$

where Z_{ref}^i and Z_{ref}^j are reference impedances of the ports i and j.

In analogy to (2.41), one can introduce the special notation T^0 to describe the cascade matrix:

$$\begin{bmatrix} b_{01} \\ a_{01} \end{bmatrix} = T^0 \begin{bmatrix} a_{02} \\ b_{02} \end{bmatrix}, \tag{2.43}$$

where $T = T_0$ if $Z_{ref}^i = Z_0^i$ for each ith port.

2.3.5 Change of Reference Impedance

The relationship between the pseudo-wave amplitudes for different reference impedances Z_{ref}^n and Z_{ref}^m results from equations (2.33) - (2.36) as:

$$\begin{bmatrix} a(Z_{ref}^n) \\ b(Z_{ref}^n) \end{bmatrix} = Q^{ij} \begin{bmatrix} a(Z_{ref}^m) \\ b(Z_{ref}^m) \end{bmatrix}, \tag{2.44}$$

where

$$Q^{nm} \equiv \frac{1}{2Z_{ref}^m} \left| \frac{Z_{ref}^m}{Z_{ref}^n} \right| \sqrt{\frac{\Re(Z_{ref}^n)}{\Re(Z_{ref}^m)}} \begin{bmatrix} Z_{ref}^m + Z_{ref}^n & Z_{ref}^m - Z_{ref}^n \\ Z_{ref}^m - Z_{ref}^n & Z_{ref}^m + Z_{ref}^n \end{bmatrix}. \tag{2.45}$$

As stated in [21], (2.44) and (2.45) are an exact expression of the complex impedance transformation. Therefore, the pseudo-waves can be accurately referred to as impedance-transformed traveling waves.

Q^{nm} can be re-written for the complex impedance transformation of reflection coefficients:

$$Q^{nm} = \sqrt{\frac{1 - j\frac{\Im(Z_{ref}^m)}{\Re(Z_{ref}^m)}}{1 - j\frac{\Im(Z_{ref}^n)}{\Re(Z_{ref}^n)}}} \frac{1}{\sqrt{1 - \Gamma_{nm}^2}} \begin{bmatrix} 1 & \Gamma_{nm} \\ \Gamma_{nm} & 1 \end{bmatrix}, \tag{2.46}$$

where:

$$\Gamma_{nm} \equiv \frac{Z_{ref}^m - Z_{ref}^n}{Z_{ref}^m + Z_{ref}^n}. \tag{2.47}$$

Finally, the reflection coefficient is transformed by:

$$\Gamma(Z_{ref}^n) = \frac{\Gamma_{nm} + \Gamma(Z_{ref}^m)}{1 + \Gamma_{nm}\Gamma(Z_{ref}^m)}. \tag{2.48}$$

Marks and Williams gave some useful examples of transferring reflection coefficients of ideal open, short and load standards. In fact, the open and short have a unique physical manifestation: their reflection coefficients are independent from the reference impedance.

2.3.6 Two-Port Reference Impedance Transformation

A simple way to transform the impedance for a two-port S-parameter matrix is to compute the associated cascade matrix T, transform it to the new reference impedance and convert results back to the S-parameter matrix. The important relationship of:

$$\begin{bmatrix} b(Z_{ref}^{n}) \\ a(Z_{ref}^{n}) \end{bmatrix} = Q^{nq} \begin{bmatrix} b(Z_{ref}^{q}) \\ a(Z_{ref}^{q}) \end{bmatrix} \tag{2.49}$$

leads to:

$$T^{pq} = Q^{pm} T^{mn} Q^{nq}. \tag{2.50}$$

The last equation shows the transformation path of the reference impedance of port 1 from Z_{ref}^{m} to Z_{ref}^{p} and for port 2 from Z_{ref}^{n} to Z_{ref}^{q}. This is the general case where both ports have different reference impedances. In most practical situations, both ports of a device use equal reference impedances. So, (2.50) simplifies to:

$$T^{pp} = Q^{pm} T^{mm} Q^{mp} = \frac{1}{1-\Gamma_{pm}^{2}} \begin{bmatrix} 1 & \Gamma_{pm} \\ \Gamma_{pm} & 1 \end{bmatrix} T^{mm} \begin{bmatrix} 1 & -\Gamma_{pm} \\ -\Gamma_{pm} & 1 \end{bmatrix}. \tag{2.51}$$

The last equation is used very often when performing the transformation of wafer-level calibration results from calibration reference impedance to measurement reference impedance (see Chapters 3, 4, and 5).

2.3.7 Load Impedance

The load impedance is defined as:

$$Z_{load} \equiv \frac{v}{i} \tag{2.52}$$

at the reference plane at which the electromagnetic waves propagates only as a single mode. The load impedance is independent from the reference impedance, similar to v and i. However, [21] states that Z_{load} is not a unique property of a one-port itself. Unlike the low-frequency circuit theory, Z_{load} depends on the fields of the mode upon it. Loading the same one-port on different waveguides or on different modes of the same waveguide may give very different results for Z_{load}.

From previously defined equations (2.34) and (2.52) follows:

$$b(Z_{load}) = 0 \text{ and } \Gamma(Z_{load}) = 0 \tag{2.53}$$

when the reference impedance Z_{ref} is equal to the load impedance Z_{load}. In this case, the impedance looks like a perfect match and its reflection coefficient vanishes. The reverse statement is relevant for the system calibration and, unfortunately, is often misunderstood: assuming that the reflection coefficient cancels out when a certain load is connected to the waveguide, the reference impedance is effectively set to $Z_{ref} = Z_{load}$. This may contradict the initial goal, especially if the load impedance is complex. Fig. 2.4 impressively demonstrates such a case. Here, the reflection coefficient of the same open element (probes in air) is measured with respect to three different LRM calibration runs. Calibrations were made using the same set of standards but with different overlaps of the probes on the planar load of 0 µm, 25 µm, and 50 µm. This led to a broad variation of the equivalent reactance of the load standard and, finally, to different calibration reference impedances [26]. A similar case is when calibrating with asymmetrical load standard that is shown in Chapter 6.

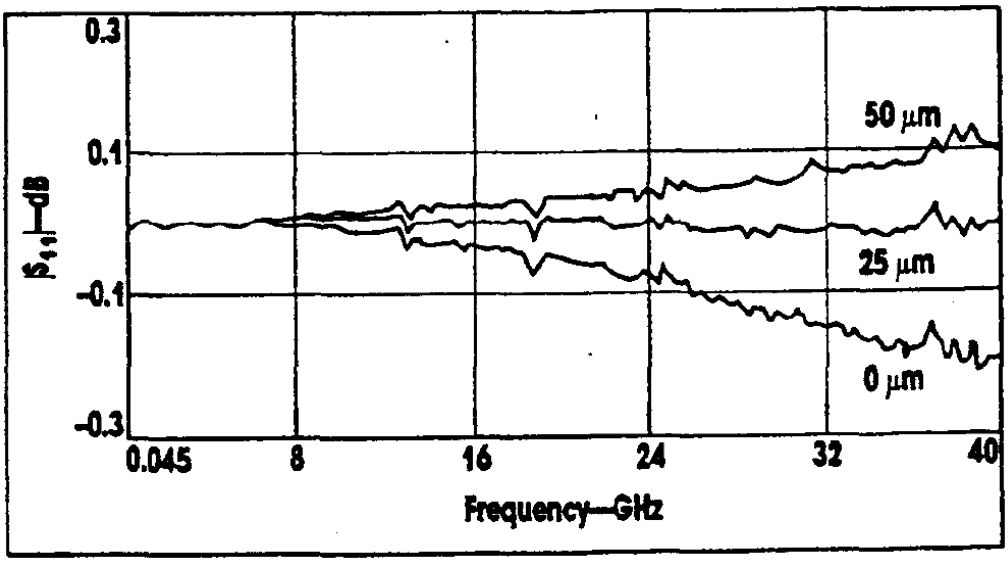


Fig. 2.4: Reflection coefficient of the planar open standard corrected by probe tip LRM calibration. The probe placement on the planar load standard affects the LRM calibration accuracy (reference impedance). Picture from [26].

From (2.53), (2.47) and (2.48), we get:

$$\Gamma(Z_{ref}) = \frac{Z_{load} - Z_{ref}}{Z_{load} + Z_{ref}}, \tag{2.54}$$

or, when solved for Z_{load}:

$$Z_{load} = Z_{ref}\frac{1 + \Gamma(Z_{ref})}{1 - \Gamma(Z_{ref})}. \tag{2.55}$$

These two equations represent the general case. They are turning into the widely-used original waveguide circuit theory equations (e.g. from [19]) when the reference impedance Z_{ref} is equal to the characteristic impedance Z_0.

The (2.55) was used to calculate the equivalent impedance of the custom load standard at the middle of a custom thru standard with the characteristic impedance Z_{LINE} different from the desired calibration reference impedance (see Chapter 3 and Chapter 4).

2.4 S-Parameter Measurement

The measurement of RF and microwave characteristics of a network is a crucial part of the development, optimization and production cycles of high-frequency components and systems. The characterization of a linear DUT in the frequency domain is carried out by the vector network analyzer (VNA). Vector network analysis technique accounts over 50 years of history [27]. Starting from simple test sets assembled and manually operated by RF engineers in the late 1950s, it has been developed to highly-sophisticated automated measurement systems that cover frequency ranges from a few tens of kHz up to THz (e.g. [28-30]).

The basic measurement concept implemented in modern VNA remains the same for all frequencies: it measures the incident a_i, reflected and transmitted b_i wave quantities at the ith port of the DUT (Fig. 2.5).

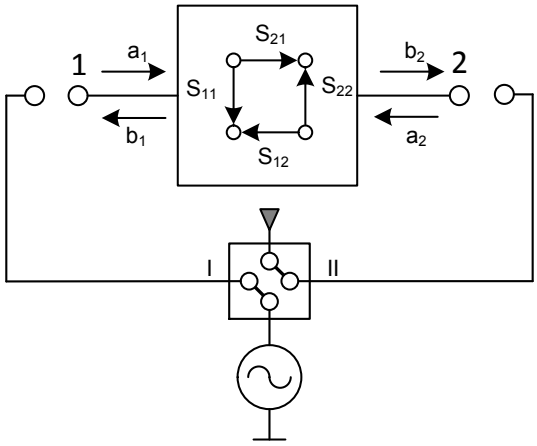


Fig. 2.5: A basic measurement concept of S-parameters realized in modern VNA

In a general way, VNA allows measurement and computation of S-parameters of the DUT in a system reference impedance, typically at 50 Ω. The incident signals are generated by the internal source, while the reflected and transmitted signals are measured by receivers. The VNA has an internal switch to redirect the incident signal (positions I and II Fig. 2.5). So, the DUT can be automatically measured in both forward and reverse directions without reconnecting. The S-parameter matrix of the DUT is computed as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{2.56}$$

where

$$S_{11} = \frac{b_1}{a_1}\Big| a_2 = 0 \ , \ S_{21} = \frac{b_2}{a_1}\Big| a_2 = 0 \tag{2.57}$$

for forward direction (when $a_2 = 0$), and

$$S_{12} = \frac{b_1}{a_2}\Big| a_1 = 0 \ , \ S_{22} = \frac{b_2}{a_2}\Big| a_1 = 0 \tag{2.58}$$

for reverse direction (when $a_1 = 0$).

Modern VNAs realize different receiver concepts (reference channel and double reflectometer), have two and more measurement ports, and can apply single-ended and true differential incident signals to the DUT (e.g. [31]).

2.5 Systematic Measurement Errors and S-parameter calibration

In [32], I presented a detailed investigation of the history and the state-of-the-art of VNA measurements and S-parameter calibration techniques (Attachment 12). My co-author, Nick Ridler from NPL (UK) added metrological aspects, such as the definition of measurement traceability, measurement assurance as well as clarification of the term “calibration” that, in fact, has multiple meanings for vector network analysis.

This research helped to form a strategy of how to approach the specific problem of the on-wafer calibration on silicon. It became clear that the calibration method should be based on a seven-term error model and should include a self-calibration step. The reflection coefficient of a high-reflective element (short or open) should be chosen as a free parameter as it is very hard to simulate or measure it for custom standards at mm-wave frequencies.

2.6 *S*-parameter Measurements at the Wafer-Level

Characterizing the un-packaged DUT at the wafer-level requires a complex measurement system with several components: VNA, Source Monitor Unit (SMU), the probe station, cables and wafer probes. The probe station provides the positioning of the test wafer with DUT, while the wafer probes convert the measurement signal from

the 3D transmission media (RF cables or rectangular waveguides) to the quasi-2D coplanar DUT interface (Fig. 2.6).

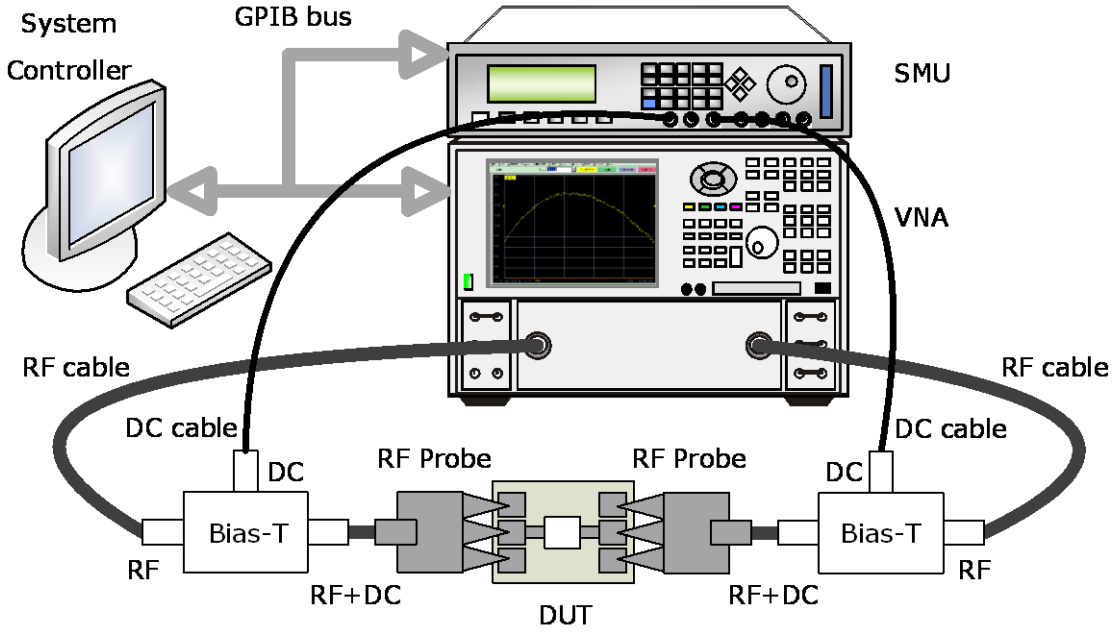


Fig. 2.6: A schematic representation of a measurement system for device characterization at the wafer-level.

2.6.1 Design of Modern Wafer Probes

There are several configurations of probe tips: Ground-Signal (GS or SG), Ground-Signal-Ground (GSG) for single-ended measurements, as well as various combinations of signal and ground contacts for dual/differential measurements (such as GSGSG, GSSG, SGS, etc.).

The wafer probe itself should carefully match the characteristic impedances Z_0 of the transmission media and provide proper conversion of the electromagnetic energy between different propagation modes. The conversion of the EM-field pattern is maintained by several RF transition steps within a single probe assembly. A conventional RF probe consists of the following parts:

1. Test instrumentation interface (coaxial or waveguide);
2. Transition from the test interface to the micro-coax cable;
3. Transition from micro-coax cable to a planar waveguide, such as CPW or microstrip;
4. Coplanar interface to a DUT on the wafer (or probe tip).

Several probes either combine steps 3 and 4 or do not use the micro-coax cable (Fig. 2.7). A coaxial connector is a commonly used test system interface of RF probes below

65 GHz. Both coaxial and waveguide connections are possible interfaces for the frequency range from 50 GHz to 110 GHz. Broadband measurement systems covering a frequency range from DC to 110 GHz in a single sweep utilize the smallest size (1 mm) coaxial connector [28-30]. Rectangular waveguides of different dimensions interface to the measurement system from above 110 GHz.

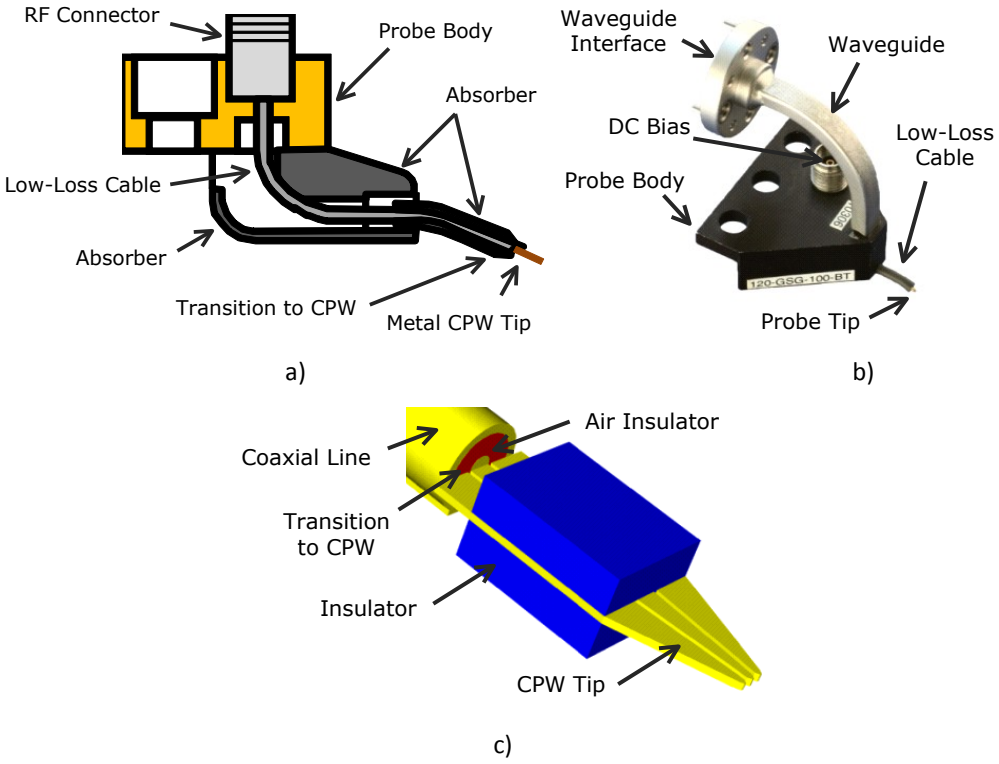
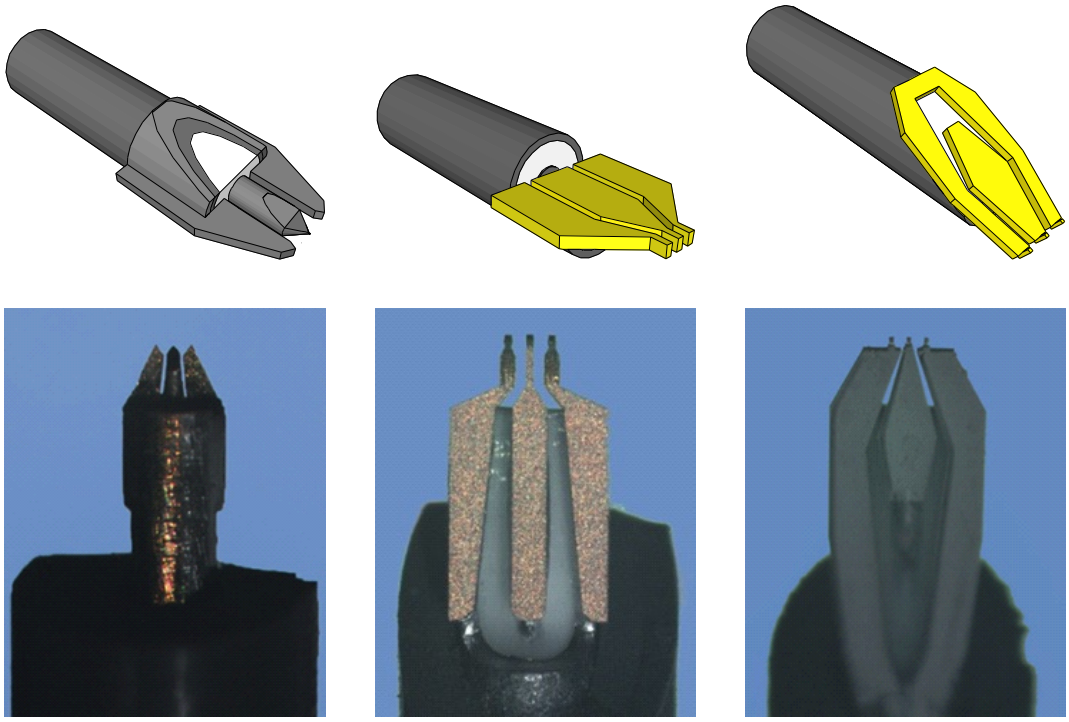


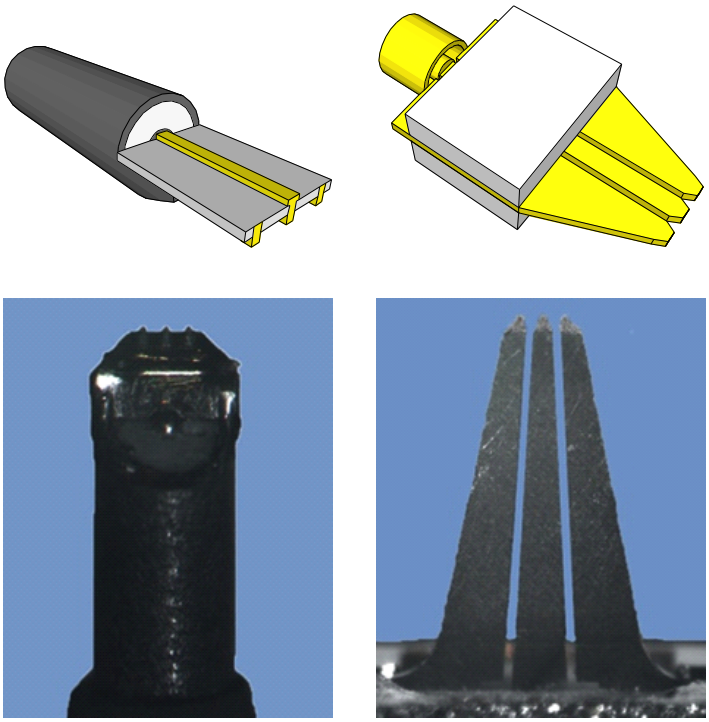
Fig. 2.7: A concept of RF probe: based on a micro-coax cable for coaxial (GGB, ACP, Allstron, top left) and waveguide (GGB, ACP, Infinity) interface (top right) and direct transition from the coaxial to the coplanar line (|Z|-Probe) (bottom).

Recently, the 0.8 mm coaxial connector was introduced for a measurement system covering a band from 70 kHz to 145 GHz in a single sweep. The 0.8 mm connector-based RF probe is also underway [33].

At mm-wave frequencies, the rectangular waveguide TE_{10} EM fields can be converted into coplanar TEM-type EM fields either directly or in two steps. The two-step method applies a short section of a micro-coax cable and is common for RF probes up to 325 GHz. The use of a micro-coax cable is advantageous from the mechanical point of view. However, its relatively high insertion loss together with the impact of additional transition step reduces the overall probe electrical performance. The direct transition to a microstrip membrane tip [34] or a micro-machined silicon CPW [35] makes the micro-coax cable dispensable.



a) b) c)



d) e)

Fig. 2.8: Design concept and photograph of various Ground-Signal-Ground probe tips, bottom view, from left to right (top): (a) Picoprobe (photo of the tip from the top), (b) ACP, (c) Allstron. On the bottom: (d) Infinity Probe (design concept shows the tip from the top), (e) |Z| Probe. All photographs are of the same magnification.

There are several approaches how to design probe tips and how to attach them to the rest of the probe (Fig. 2.8):

1. The signal conductor of the micro-coax cable is shaped out to form the signal tip. Ground blades of the tip are soldered from both sides of the cable (Picoprobe, GGB);
2. The air-isolated CPW tip is attached to the micro-coax cable (ACP, Cascade Microtech and Allstron Probes);
3. The flexible polyamide microstrip line, that ends with the CPW tips, is attached to the micro-coax cable (Infinity Probe, Cascade Microtech);
4. Direct transmission (without micro-coax cable) from the coaxial connector to the air-isolated CPW contacts (|Z|-Probe, Rosenberger-Cascade Microtech);
5. Direct transmission from the rectangular waveguide to a polyamide microstip line (500 GHz Infinity Probe, Cascade Microtech);
6. Direct transition from the rectangular waveguide to a micro-machined silicon CPW contact structure (DMPI, (Fig. 2.9).
7. This variety of design concepts roots in a tradeoff between mechanical and electrical requirements for probing on different contact pad materials. The interfaces, in particular the probe tip, bring discontinuities into the measurement signal path. As per [21], such discontinuity causes the generation of higher order propagation modes *per se.* Thus, wafer probes and DUT launches must support only a single quasi-TEM propagation mode and should exclude higher-order modes or exhibit a significantly higher impedance to them (e.g. [36]).

The impact of the probe design on the calibration residual errors and the measurement accuracy is discussed later in Chapter 9.

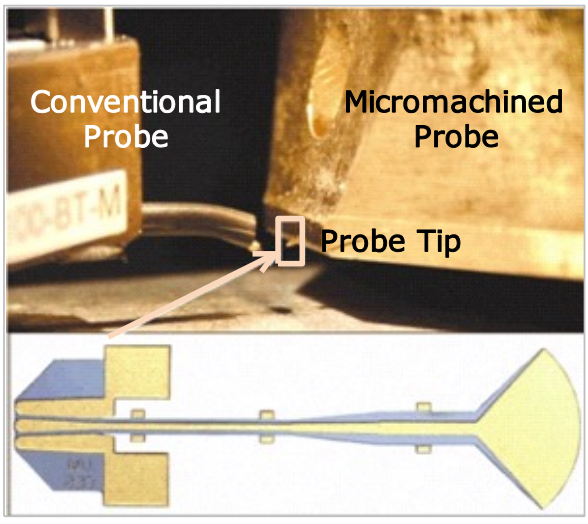


Fig. 2.9: Ground-Signal-Ground probe tip of the DMPI probe. Picture from [17].

2.6.2 DUT Contact Pads and BEOL Parasitics

The size of an elementary device (i.e. a transistor) of advanced mm-wave technologies is just a few micrometers. It is not possible to contact it directly even using RF probes with the smallest available pitch (distance between signal and ground) of 50 µm. Moreover, active devices from advanced semiconductor processes are covered by many layers of BEOL metallization. The BEOL "device infrastructure" includes the probe contact pads, interconnect lines and via stacks. The impact of the BEOL parasitic impedance became a substantial problem for high-performance devices at higher measurement frequencies: the parasitics are several orders of magnitude larger than the intrinsic parameters of the device (see also Fig. 1.5).

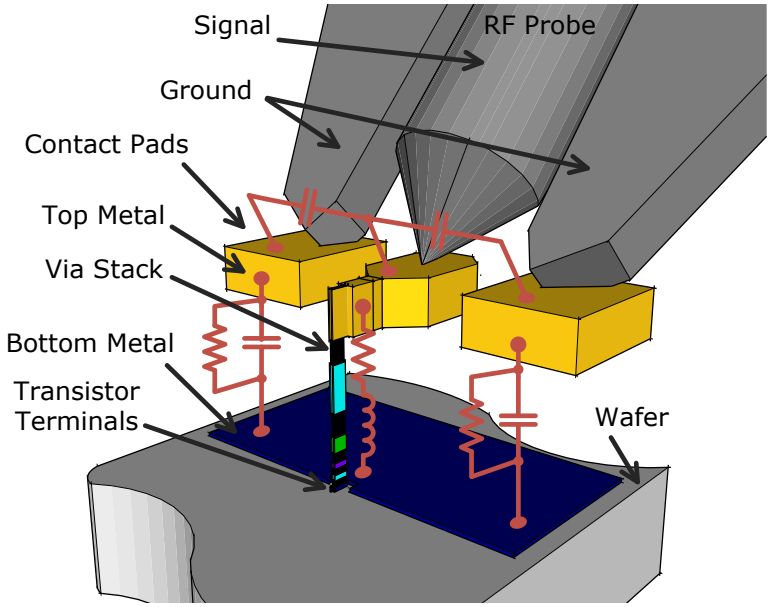


Fig. 2.10: An example of a ground-signal-ground pads and probe, and simplified presentation of the BEOL parasitic circuit elements of a DUT.

Therefore, the "intrinsic device" must be de-embedded from the surrounding parasitics of the BEOL and pads of a "total device". De-embedding is the second step of the calibration process. It uses special structures that are often called de-embedding "dummies". They are laid out similar to the device and, therefore, represent the DUT BEOL parasitics. Dummies are measured in the same series as the DUT. The measured parasitics are subtracted from the "total device" yielding the characteristics of the intrinsic device.

There are different ways and complexity orders of de-embedding depending upon the measurement application, the design of the DUT, measurement parameters, and the frequency range. It can be applied to passive (inductors, capacitors, and resistors), as well as active devices (transistors, diodes, etc.). Because substrate parameters (such as resistivity, oxide thickness, etc.) vary across the wafer, dummy structures should be located near to the DUT.

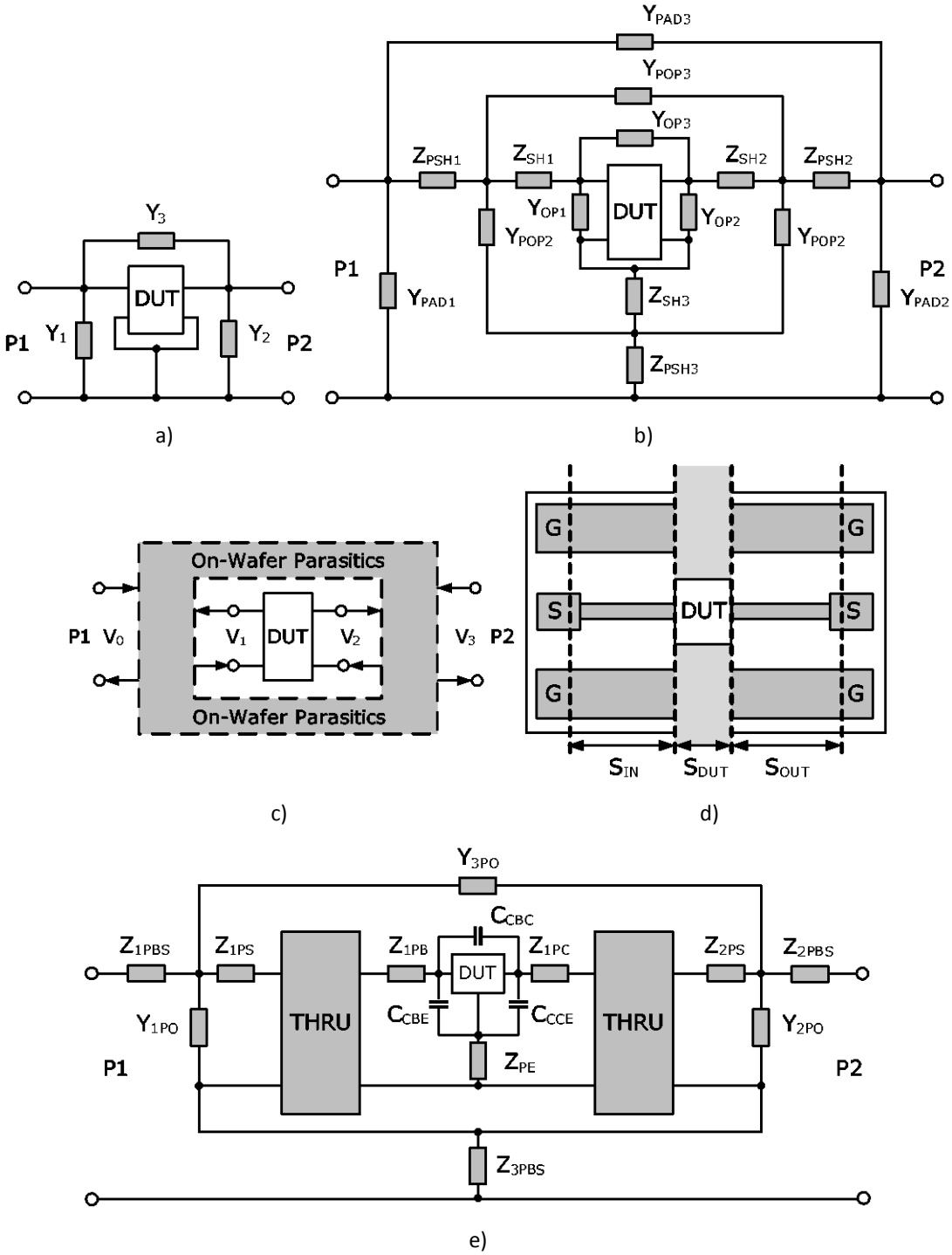


Fig. 2.11: Representation of the BEOL parasitics by different de-embedding methods: two-step (a), five-step (b), general 4-four-port (c), transmission line-based (d) and the scalable six-step (e).

The increase of the complexity of the semiconductor process, the operation frequency of the device, and the demand for improvement of the accuracy of device characterization and modeling pushed the development of the de-embedding procedures. In 1987, Van Wijnen introduced the two-step open short de-embedding procedure for characterization of Si BJTs up to 18 GHz. Since then, semiconductor

processes, device maximum operation frequencies, and, consequently, de-embedding methodology have made a substantial progress. Today, many advanced de-embedding procedures have been proposed, such as the lumped-element based five-step method (proved up to 50 GHz, [37]), a general 4-port de-embedding (proven up to 110 GHz, [38]), the scalable 6-step method (proved up to 110 GHz, [39]) or the transmission line based method (proven up to 170 GHz, [40]). Fig. 2.11 compares how DUT backend parasitics are captured by different de-embedding algorithms over different equivalent circuits.

With the increase of measurement frequencies and the decrease of the size of an elementary device, de-embedding of the BEOL parasitic effects became a very complex process. It requires comprehensive equivalent circuits, more dummy elements, as well as multiple measurement and calculation steps. Numerous additional sources of errors occur leading to common mistakes, such as under- or over-de-embedding.

In Chapter 7, it will be shown that the implementation of the *in-situ* calibration approach captures the largest portion of the BEOL parasitics within one calibration step. The remaining parasitics are of lumped nature. They can easily be described by a simple model and calculated out using a two-step de-embedding method even at mm-wave frequencies.

2.6.3 Calibration Standards

For the wafer-level measurements, the “calibration standard” term is applied to an element with fully (or partly) known electrical characteristics, such as impedance Z of reflection elements and characteristic impedance Z_0 and propagation constant γ, for transmission (line) elements. These elements are often realized in the coplanar waveguide (CPW) design and accumulated on an alumina substrate, also called “Calibration Substrate” or Impedance Standard substrate (ISS, Fig. 2.12, Fig. 2.13). Such standards are used for the probe calibration process when the measurement reference plane is set near to the probe tip end (Fig. 2.14).

An alternative approach is to fabricate calibration standards together with the DUT on the same media. They share the same design with the DUT (microstrip or CPW) and are located close to it. Wafer-embedded reference elements are usually called “on-wafer” standards to emphasize the difference to the ISS standards, which are fabricated on a different media, or “off-wafer”.

On-wafer calibration is a common practice for III-Vs semiconductor technologies. Implementing on-wafer standards on silicon is challenging and less common due to high substrate loss and its frequency-dependent conductivity. Fig. 2.15 gives an example of the on-wafer TRL kit implemented on 65 nm CMOS process for characterization of a power amplifier from 140 GHz up to 220 GHz [41].

Chapters 4-6 discuss the on-wafer implementation of the multiline TRL and the transfer TMR calibration methods for advanced CMOS and BiCMOS technologies. It is also shown that the electrical parameters of commercial calibration standards strongly depend on the material the calibration substrate was placed on (Chapter 9).

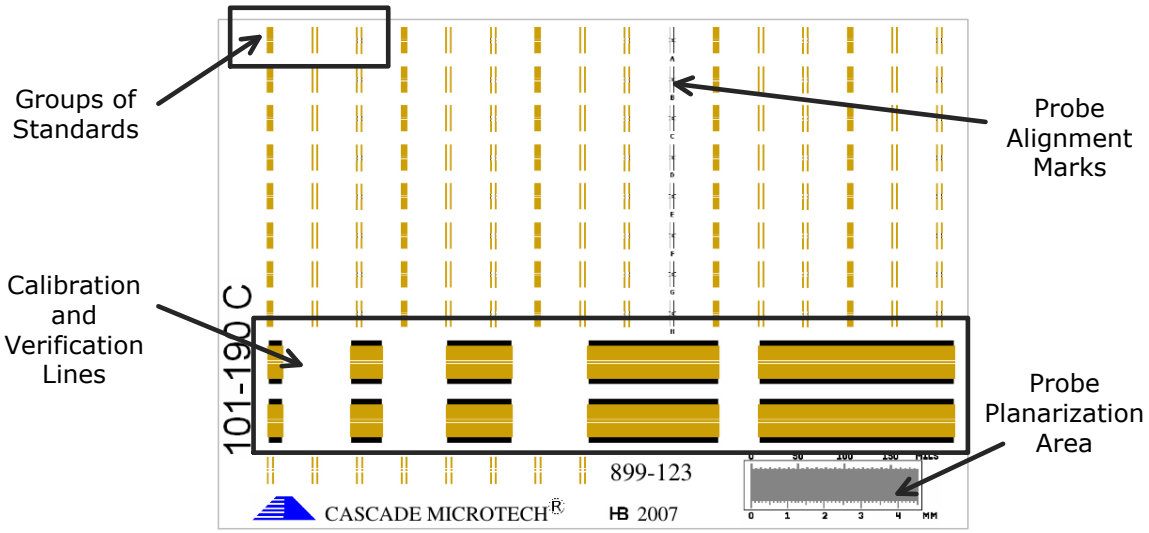


Fig. 2.12: Example of commercially available calibration substrate that includes lumped-element impedance standards, calibration and verification lines, probe alignment marks as well an area for probe planarization.

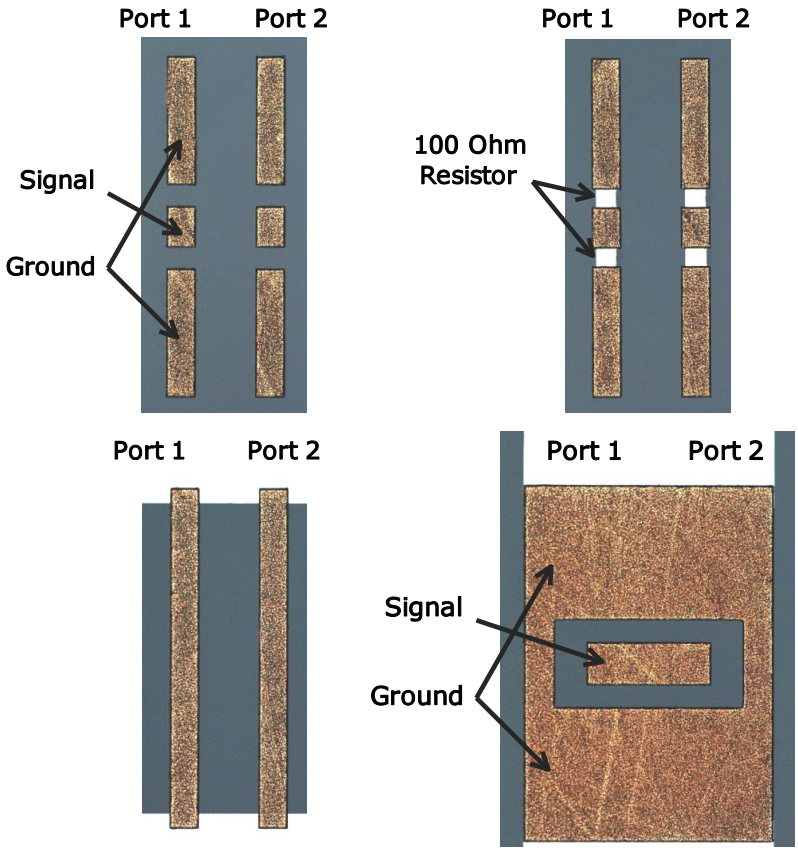


Fig. 2.13: Example of commercially available off-wafer coplanar calibration standards (from left to right): paired opens, paired loads, paired shorts, and the thru. Such standards are used for most popular wafer-level calibration procedures.

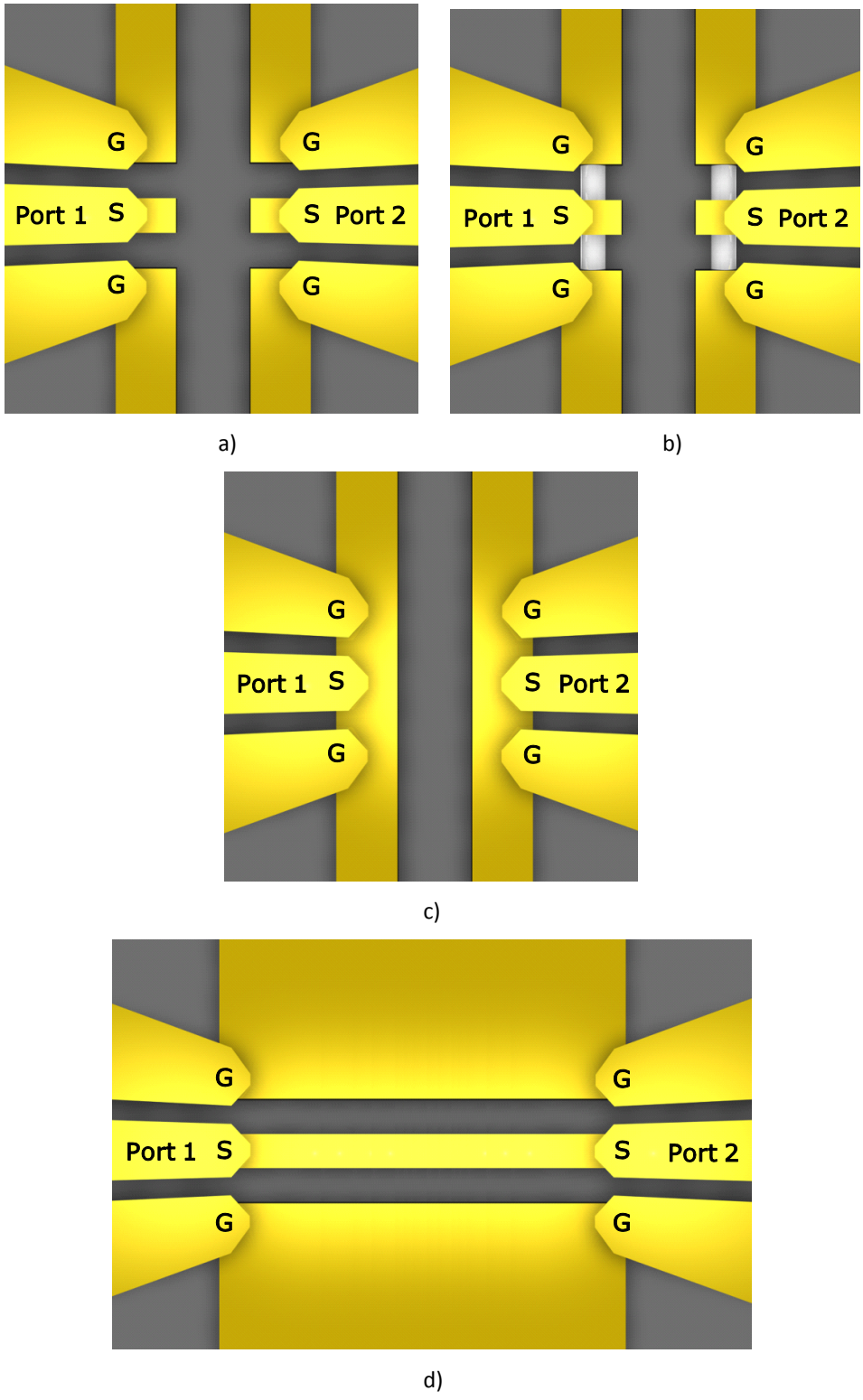


Fig. 2.14: Example of the probe tip calibration. RF probe contacting the CPW commercial standards: open (a), load (b), short (c), and line (d)

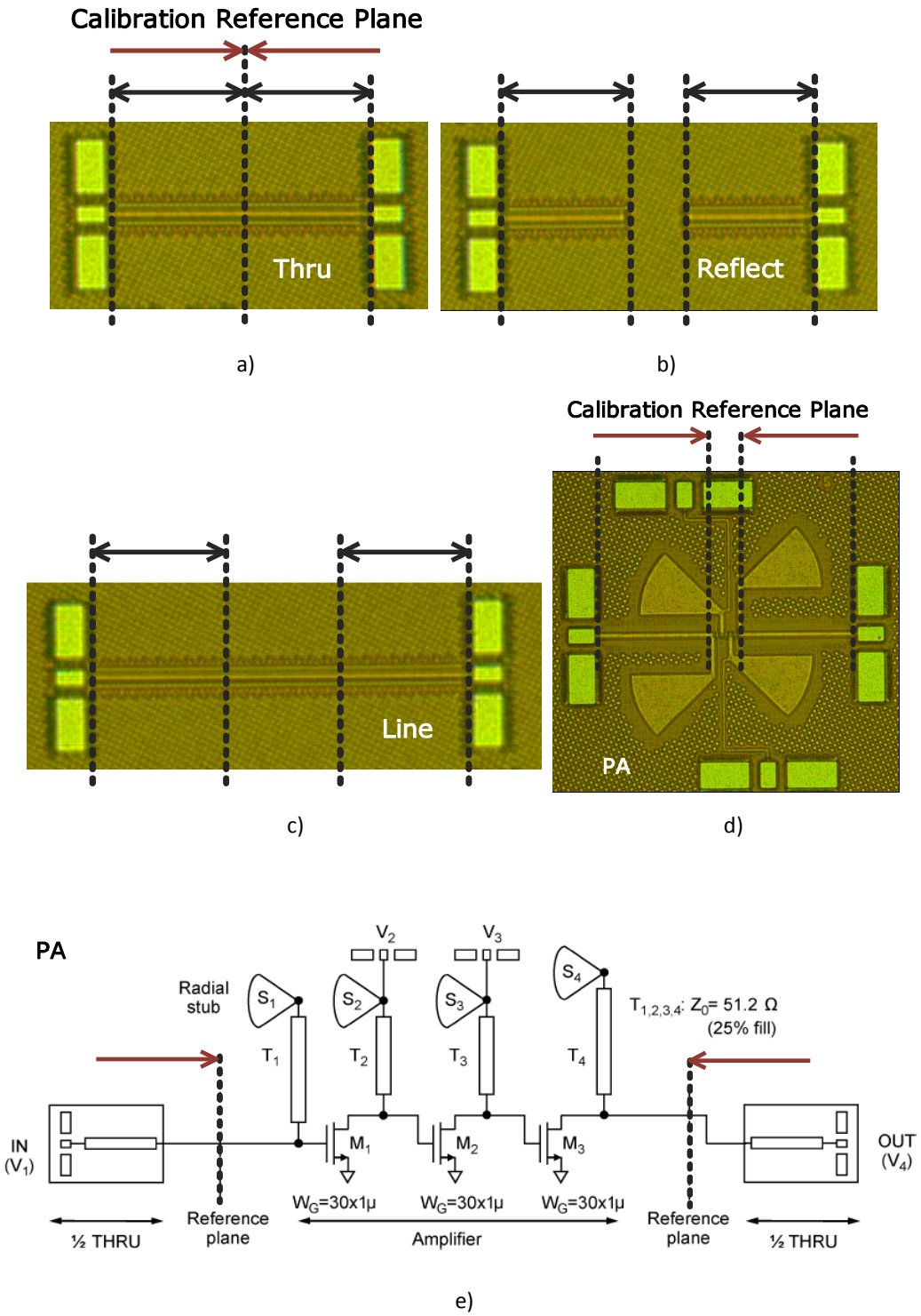


Fig. 2.15: Example of the on-wafer TRL calibration kit design for measurements of CMOS PA: the thru (a), the reflect (b), and the line (c) calibration standards, the test power amplifier (d) and (e). Pictures are from [41].

3 DEVELOPMENT OF CALIBRATION SOLUTIONS

3.1 Requirements

On-wafer RF measurement requires the shift of the S-parameter measurement reference plane either to the probe tip end or to a certain virtual on-wafer location close to the terminals of the intrinsic device.

Limitations of planar calibration standards require special wafer-level calibration procedures of the VNA. Conventional methods, that are developed for coaxial and/or waveguide environment may lead to significant calibration and measurement errors at the wafer level especially at higher frequencies [42]. The need for accurate and consistent measurement results pushed engineers to develop dedicated wafer-level calibration techniques, such as LRRM [25], the NIST multiline TRL [43] and the translate LRM [44].

Silicon application, however, raises additional calibration challenges. The key requirements to on-wafer calibration on silicon are:

1. Accuracy. Sensitivity of a calibration method to non-ideal characteristics of custom standards limits its accuracy. In contrast to the probe-tip calibration, on-wafer calibration is an in-line step. It is hard or impossible to trim standards to the desired performance in the same way as the ISS elements. Calibration methods should be insensitive to non-ideal standards;
2. Minimal test chip size. Standards are embedded on every test chip together with devices. In contrast to the III-V's, silicon is mostly used for RF consumer applications. Minimal size of calibration chips is mandatory to save the on-wafer real estate and reduce test and manufacturing cost of the final product;
3. Same geometry with the DUT. The design of standards should match the geometry of the DUT (for elementary devices).
4. Reduction of the cost of test. Between the calibration and device measurement steps, there should be no operator interaction, like re-positioning of probes. Calibration should be run automatically and without need for motorized RF positioners.

3.2 Calibration of a Two-Port VNA

Analyzing calibration theory and specifics of advanced silicon processes led to the conclusion that the transfer TMR self-calibration method was the best candidate for application at the device production environment, while the multiline TRL could serve as the benchmark, e.g. for the process development and integration cycle. Conventional LRM sets the calibration reference impedance to the impedance of the load standard. The impedance of a planar load is, in general, complex with the load resistance $R_{LOAD} \neq 50\ \Omega$ [44, 45]. In result, the calibration reference impedance is complex, frequency dependent and difficult to define. Interpretation of the S-parameters measured with respect to such calibration conditions is a very hard task (see Chapter 2).

The concept of TMR was presented by Eul and Schiek in 1988 [46]. Later, they showed how TMR can be derived from the general Txx algorithm [47]. The match standard of TMR is a double-one port that is perfectly matched to the system reference impedance. Thus, its reflection coefficient r_M should satisfy $r_M = 0$ in the calibration reference impedance and its pseudo S-parameters should vanish (the situation that was discussed in Chapter 2). Such conditions usually hold for coaxial applications.

Obviously, another solution for TMR is needed to relax requirements to the match standard regarding two aspects:

1. Enable the use of complex impedance elements;
2. Abolition of $S_{X2,11} = S_{X2,22}$ ([48], Table 3.1).

TMR that enables such conditions is often called “transfer TMR” [49]. The impedance of the match standard can be defined at each measurement port and can be arbitrary. This is the most common scenario for a custom load standard implemented on a silicon test chip.

Table 3.1: Conditions of Transfer TMR Calibration.

Standards	Requirements	Unknown	Terms	Product
Thru	Known: S_{11}, S_{21}, S_{12}, S_{22}	n/a	4	n/a
Match	Known: S_{11}, S_{22}	n/a	2	n/a
Reflect	S_{11}=S_{22} known within ±90 degree	S_{11} (S_{22})	1	r_X S_{11}=S_{22}

To the best of my knowledge, the complete mathematical solution for the transfer TMR has never been published. That is why it was re-derived and is presented in the next section. This derivation is the key to the solution when the calibration reference

impedance, the characteristic impedance of the thru standard, as well as the impedances of the paired match are all different.

3.3 Transfer TMR Solution

Fig. 3.1 shows the seven-term systematic error model of a two-port double reflectometer VNA. Here, m are the ideal measurement receivers, a and b are the incident and reflected/ transmitted waves respectively, $[A]$ and $[B]$ are the 2x2 matrices of error terms, $[T_X]$ is the DUT matrix of transmission T-parameters.

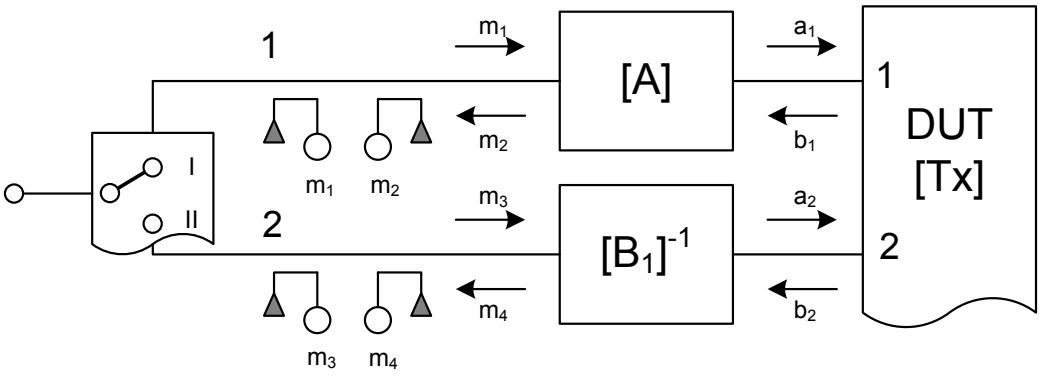


Fig. 3.1: The seven-term systematic error model of a two port double reflectometer VNA.

As it was demonstrated in [47], the relationship between the measured wave quantities m and the wave quantities at the DUT terminal a and b can be fully described by the matrix equation:

$$\begin{bmatrix} m_1 \\ m_2 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} b_1 \\ a_1 \end{bmatrix} \tag{3.1}$$

It is important to note, that matrix $[A]$ represents the so-called error box and does not correspond to any physical two-port element. As stated in [49], such nomenclature is chosen for calculation convenience as well as for accordance with previously published materials.

For the case of a one-port measurement of a DUT with the reflection coefficient:

$$r_X = \frac{b_1}{a_1}, \tag{3.2}$$

equation (3.1) can be transformed to:

$$\frac{m_1}{m_2} = \frac{A_{11} r_X + A_{12}}{A_{21} r_X + A_{22}} \tag{3.3}$$

Equation (3.3) is the fundament of the one-port calibration and error correction.

It is easy to show, that for the error correction step, elements of matrix $[A]$ can be defined up to one common constant factor α. The last allows normalization of the terms of $[A]$ to one arbitrary parameter. It is convenient to set the normalization factor to A_{22}. For simplification, the notation A_{ij} is further used for the normalized elements, too. With this assumption, (3.3) can be re-written to:

$$\frac{m_1}{m_2} = \frac{A_{11} r_X + A_{12}}{A_{21} r_X + 1} \tag{3.4}$$

Similar to the first reflectometer, the second reflectometer can be described by:

$$\begin{bmatrix} m_3 \\ m_4 \end{bmatrix} = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \tag{3.5}$$

The same assumption as for $[A]$ holds for the matrix $[B]$, too: it is a virtual two-port error box element. Addressing the way how it is connected, equation (3.5) is linearly transformed to:

$$\begin{bmatrix} a_2 \\ b_2 \end{bmatrix} = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix}^{-1} \begin{bmatrix} m_3 \\ m_4 \end{bmatrix} \tag{3.6}$$

Taking into account that the transmission matrix of a two-port DUT $[T_X]$ is given by:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{X11} & T_{X12} \\ T_{X21} & T_{X22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \tag{3.7}$$

and with respect to (3.1) and (3.6), we get the mathematical description of a two-port measurement system:

$$\begin{bmatrix} m_1 \\ m_2 \end{bmatrix} = [A][T_X][B]^{-1} \begin{bmatrix} m_3 \\ m_4 \end{bmatrix} \tag{3.8}$$

Equation (3.8) establishes the relationship between the actual DUT parameters, represented by the transmission matrix $[T_X]$ and the wave quantities m_i measured by the ideal VNA receivers over the error matrixes $[A]$ and $[B]^{-1}$ (Fig. 3.1).

Modern VNAs automatically measure the DUT in both directions (Fig. 2.5). Thus, (3.8) can be extended to:

$$\begin{bmatrix} m_1' & m_1'' \\ m_2' & m_2'' \end{bmatrix} = [A][T_X][B]^{-1} \begin{bmatrix} m_3' & m_3'' \\ m_4' & m_4'' \end{bmatrix} \tag{3.9}$$

or, in short form:

$$[M_X] = [A][T_X][B]^{-1} \tag{3.10}$$

where $[M_X]$ is the measurement matrix, given by:

$$[M_X] = \begin{bmatrix} m'_1 & m''_1 \\ m'_2 & m''_2 \end{bmatrix} \begin{bmatrix} m'_3 & m''_3 \\ m'_4 & m''_4 \end{bmatrix} = [m_a][m_b]^{-1} \tag{3.11}$$

The primed m'_i correspond to the forward, while double-primed m''_i correspond to the reverse measurement directions. Equation (3.11) also proves that the bidirectional switch which leads the incident measurement signal is excluded from the measurement matrix reflectometer VNA architecture: it does not require a high-quality switch with high repeatability and isolation.

As it was shown in [47], the error-term matrixes $[A]$ and $[B]$ can be derived from three different standards:

$$[M_1] = [A][T_{X1}][B]^{-1} \tag{3.12}$$

$$[M_2] = [A][T_{X2}][B]^{-1} \tag{3.13}$$

$$[M_3] = [A][T_{X3}][B]^{-1} \tag{3.14}$$

The first standard, the thru, is a perfectly matched, zero-length transmission element. Its transmission matrix is given by:

$$[T_1] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3.15}$$

Now, the measurement matrix for this standard according to (3.11) is:

$$[M_1] = \begin{bmatrix} m'_{11} & m''_{11} \\ m'_{21} & m''_{21} \end{bmatrix} \begin{bmatrix} m'_{31} & m''_{31} \\ m'_{41} & m''_{41} \end{bmatrix} = [m_{a1}][m_{b1}]^{-1} \tag{3.16}$$

From the measurements of the first (r_M) and second (r_R) reflection standards follows:

$$\frac{m'_{12}}{m'_{22}} = \frac{A_{11}r_{M1} + A_{12}}{A_{21}r_{M1} + A_{22}} = \Gamma_{A1} \tag{3.17}$$

$$\frac{m''_{32}}{m''_{42}} = \frac{B_{11} + B_{12}r_{M2}}{B_{21} + B_{22}r_{M2}} = \Gamma_{B1} \tag{3.18}$$

$$\frac{m'_{13}}{m'_{23}} = \frac{A_{11}r_{R1} + A_{12}}{A_{21}r_{R1} + A_{22}} = \Gamma_{A2} \tag{3.19}$$

$$\frac{m''_{33}}{m''_{43}} = \frac{B_{11} + B_{12}r_{R2}}{B_{21} + B_{22}r_{R2}} = \Gamma_{B2} \tag{3.20}$$

Equations (3.17) and (3.19) can be re-written as:

$$A_{11}r_{M1} + A_{12} - A_{21}r_{M1}\Gamma_{A1} - A_{22}\Gamma_{A1} = 0 \tag{3.21}$$

$$A_{11}r_{R1} + A_{12} - A_{21}r_{R1}\Gamma_{A2} - A_{22}\Gamma_{A2} = 0 \tag{3.22}$$

and (3.18) and (3.20) as:

$$B_{11} + B_{12}r_{M2} - B_{21}\Gamma_{B1} - B_{22}\Gamma_{B1}r_{M2} = 0 \tag{3.23}$$

$$B_{11} + B_{12}r_{R2} - B_{21}\Gamma_{B2} - B_{22}\Gamma_{B2}r_{R2} = 0. \tag{3.24}$$

Using (3.15), we can replace elements of matrix $[B]$ in (3.23) and (3.24):

$$[B] = [M_1]^{-1}[A] \tag{3.25}$$

and obtain:

$$A_{11}c_1 + A_{12}r_{M2}c_1 - A_{21}c_2 - A_{22}r_{M2}c_2 = 0 \tag{3.26}$$

$$A_{11}c_3 + A_{12}r_{R2}c_3 - A_{21}c_4 - A_{22}r_{R2}c_4 = 0, \tag{3.27}$$

where:

$$\begin{aligned} c_1 &= M_{1,22} + M_{1,21}\Gamma_{B1}, \\ c_2 &= M_{1,12} + M_{1,11}\Gamma_{B1}, \\ c_3 &= M_{1,22} + M_{1,21}\Gamma_{B2}, \\ c_4 &= M_{1,12} + M_{1,11}\Gamma_{B2}. \end{aligned} \tag{3.28}$$

Equations (3.21), (3.22), (3.26) and (3.27) are the basis for the self-calibration step that calculates the originally unknown reflection coefficient r_R of the reflect standard. In a short form, they can be rewritten as:

$$[C_R]\underline{[A]} = \underline{0}, \tag{3.29}$$

where:

$$\underline{[A]} = \begin{bmatrix} A_{11} & A_{12} & A_{21} & A_{22} \end{bmatrix}^T.$$

Except the trivial solution, when $\underline{[A]} = \underline{[0]}$ (what is out of our scope), equation (3.29) holds if:

$$det[C_R] = 0. \tag{3.30}$$

The last condition is used to find the missing parameter r_R. It is important to stress that:

$$r_{R1} = r_{R2} = r_R \tag{3.31}$$

must be forced, while $r_{M1} = r_{M2}$ is not required. In fact, (3.30) can also be solved when:

$$r_{M1} \neq r_{M2} \neq 0. \tag{3.32}$$

This is an essential condition that satisfies the initial requirements to the *in-situ* transfer TMR. The condition $r_M = 0$ does not need to be forced for all VNA ports (as discussed in Chapter 2).

Using (3.31) and (3.32), (3.30) yields:

$$r_R = \frac{-k_1 \pm \sqrt{k_1^2 - 4k_0k_2}}{2k_2}, \tag{3.33}$$

where:

$$k_0 = r_{M1}r_{M_2}(a_2 - a_1) + (a_3 - a_2),$$

$$k_1 = (r_{M1} + r_{M2})(a_2 - a_1) + (a_3 - a_2),$$

$$k_2 = r_{M1}r_{M2}(a_3 - a_2) + (a_2 - a_1),$$

with:

$$a_1 = c_2c_4 + c_1c_3\Gamma_{A1}\Gamma_{A2},$$

$$a_2 = c_1c_4\Gamma_{A2} + c_2c_3\Gamma_{A1},$$

$$a_3 = c_1c_4\Gamma_{A1} + c_2c_3\Gamma_{A2}$$

The right solution for the sign in (3.33) can easily be found from the estimated phase of the reflection coefficient of the reflect standard. It is sufficient to know it within ± 90 degree for each frequency point.

Now, all seven parameters of standards are known and the calibration procedure can be executed as follows. Normalizing (3.17) to A_{22}, equations (3.17) and (3.18) and can be reformed:

$$-\tilde{A_{11}}r_{M1} - \tilde{A_{21}} + \tilde{A_{21}}\Gamma_{A1}r_{M1} = -\Gamma_{A1} \tag{3.34}$$

$$-\tilde{B_{11}} - \tilde{B_{12}}r_{M2} + \tilde{B_{21}}\Gamma_{B1} + \tilde{B_{22}}\Gamma_{B1}r_{M1} = 0 \tag{3.35}$$

where:

$$\widetilde{[A]} = \begin{bmatrix} A_{11}/A_{22} & A_{12}/A_{22} \\ A_{21}/A_{22} & A_{22}/A_{22} \end{bmatrix} = \begin{bmatrix} \tilde{A_{11}} & \tilde{A_{12}} \\ \tilde{A_{21}} & 1 \end{bmatrix},$$

$$\widetilde{[B]} = \begin{bmatrix} B_{11}/A_{22} & B_{12}/A_{22} \\ B_{21}/A_{22} & B_{22}/A_{22} \end{bmatrix}.$$

From (3.19) and (3.20), two further equations can be derived:

$$-\tilde{A_{11}}r_R - \tilde{A_{12}} + \tilde{A_{21}}\Gamma_{A2}r_R = -\Gamma_{A2}, \tag{3.36}$$

$$-\tilde{B_{11}} - \tilde{B_{12}}r_R + \tilde{B_{21}}\Gamma_{B2} + \tilde{B_{22}}\Gamma_{B2}r_R = 0. \tag{3.37}$$

The measurements of the thru give additional four equations:

$$\tilde{A_{11}} - M_{1,11} - M_{1,12}\tilde{B_{21}} = 0, \tag{3.38}$$

$$\tilde{A_{12}} - M_{1,11}\tilde{B_{12}} - M_{12}\tilde{B_{22}} = 0, \tag{3.39}$$

$$\tilde{A_{21}} - M_{21}\tilde{B_{11}} - M_{22}\tilde{B_{12}} = 0, \tag{3.40}$$

$$M_{21}\tilde{B_{12}} + M_{22}\tilde{B_{22}} = 1. \tag{3.41}$$

Equations (3.34) and (3.35), the combination of (3.36) and (3.37), and equations (3.38)-(3.41) can be assembled in matrix form:

$$[C]\underline{[AB]} = \underline{[V]}. \tag{3.42}$$

And finally:

$$\underline{[AB]} = [C]^{-1}\underline{[V]}, \tag{3.43}$$

where:

$$C = \begin{bmatrix} -r_{M1} & 1 & \Gamma_{A1}r_{M1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & -r_{m2} & \Gamma_{B1} & \Gamma_{B1}r_{M2} \\ -r & -1 & \Gamma_{A2}r_R & -1 & -r_R & \Gamma_{B2} & \Gamma_{B2}r_R \\ 1 & 0 & 0 & -M_{1,11} & 0 & -M_{1,12} & 0 \\ 0 & 1 & 0 & 0 & -M_{1,11} & 0 & -M_{1,12} \\ 0 & 0 & 1 & -M_{1,21} & 0 & -M_{1,22} & 0 \\ 0 & 0 & 0 & 0 & M_{1,21} & 0 & M_{1,22} \end{bmatrix}, \tag{3.44}$$

$$\underline{[V]} = \begin{bmatrix} -\Gamma_{A1} & 0 & -\Gamma_{A2} & 0 & 0 & 0 & 1 \end{bmatrix}^T, \tag{3.45}$$

and

$$\underline{[AB]} = \begin{bmatrix} \tilde{A_{11}} & \tilde{A_{12}} & \tilde{A_{21}} & \tilde{B_{11}} & \tilde{B_{12}} & \tilde{B_{21}} & \tilde{B_{22}} \end{bmatrix}^T. \tag{3.46}$$

3.3.1 Notes on Calibration Reference Impedance

Calibration condition (3.16) requires that the characteristic impedance of the thru Z_{LINE} must be fully matched with the calibration reference impedance $Z_{REF} = 50\ \Omega$, i.e. $S_{1,11} = S_{1,22} = 0$. While it is natural for coaxial applications, satisfying this requirement remains very challenging at the wafer-level [22].

Adopting the TMR for a more general situation, such as $Z_{LINE} \neq Z_{REF}$, significantly complicates the derivation of the solution. An alternative way was proposed in [44] and then discussed in details in [21]. This approach is used at NIST for a lumped standard based calibration, widely known as “NIST LRM” or “Translate LRM”. The calibration calculations are proceeded as usual, resulting in matrices $[A]$ and $[B]$. At this step, calibration solution is defined for the reference impedance Z_{REF} equal to the characteristic impedance Z_{LINE} of the thru. Then, $[A]$ and $[B]$ are transformed to any target reference impedance Z_{REF}, using equation (2.51). However, the characteristic impedance of the thru (i.e. the source reference impedance) must be known.

3.3.2 Calibration with a Thru of a Finite Length

Due to the TMR requirement (3.16), the thru is often called the “postulated standard” of a zero length. Its measurement is nothing else than looping back the measurement system to itself. RF probes cannot be connected together the same way as coaxial cables. Instead, the wafer-level thru is realized as a short line of a given length l, the propagation constant γ, and the characteristic impedance Z_{LINE} (Fig. 2.13). Hence, and under the previously discussed conditions $Z_{REF} = Z_{LINE}$, its transmission matrix $[T_1]$ is:

$$[T_1] = \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{bmatrix} \tag{3.47}$$

Again, replacing (3.15) by (3.47) would make all further calculations very bulky. An alternative way was proposed by [47]: the calibration steps can be performed in the same way as for the TMR procedure, yielding matrixes $[A]$ and $[B]$. In this case, the calibration reference plane is set to the center of the thru standard. If required, it can be further moved to any arbitrary position. For instance, the following transformation sets the calibration reference plane to the end of the thru standard:

$$[\hat{A}] = [A][L]^{-1}, [\hat{B}] = [B][L], \tag{3.48}$$

where:

$$[L] = \begin{bmatrix} e^{-\frac{1}{2}\gamma l} & 0 \\ 0 & e^{+\frac{1}{2}\gamma l} \end{bmatrix}. \tag{3.49}$$

3.3.3 Notes on the Probe Tip Reflection Standards

Often, the impedance of the match standard r_{M1} and r_{M2} is given for the measurement reference plane at the end of the thru (e.g. at the probe tip end). This is a common situation for commercial alumina calibration substrates. As I will show later, this is the most appropriate approach for the *in-situ* standards.

For this case, both r_{M1} and r_{M2} need to be recalculated as:

$$r_0 = r_M e^{\gamma l} \tag{3.50}$$

where r_M is the reflection coefficient of the match defined at the end of the thru. l and γ are respectively the length and the propagation constant of the thru (Fig. 3.2). Furthermore, the impedance of the match r_0 should be transferred from the source impedance (typically $Z_{REF} = 50\ \Omega$) to the reference impedance $Z_{REF} = Z_{LINE}$ using (2.55).

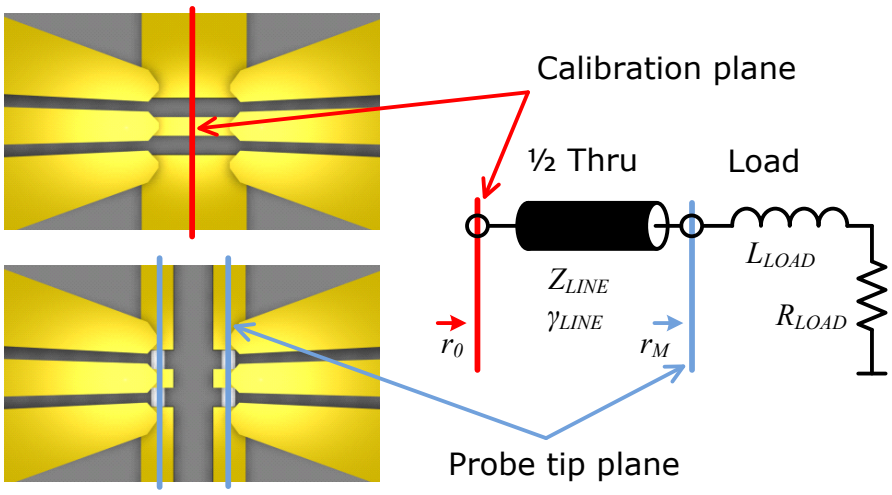


Fig. 3.2: Definition of the match reflection coefficient at the probe tip end (r_M) and at the middle of the thru standard r_0 for the transfer TMR.

A similar correction is required for the reflect standard. Its reflection coefficient r_R is given by (3.33) at the calibration reference plane, i.e. at the middle of the thru. This should be taken into account when determining the right sign of the root solution. Often, r_R is used for a quick qualitative verification of the TMR calibration accuracy (Some examples of it are given in Chapter 6). In this case, r_R needs to be transferred to the more common reference position, e.g. at the end of the thru by:

$$r'_R = r_R e^{-\gamma l}. \tag{3.51}$$

3.4 Verification of the Transfer TMR

While the concept of the transfer TMR has been known for years, the quantitative accuracy verification of this method has never been investigated. I developed a verification methodology and presented the results in [50] together with Ralf Doerner from FBH (Berlin, Germany) who made all required measurements. We shared calculation and the data analysis.

In this work, we proved the capability of the transfer TMR algorithm to accurately set the calibration reference impedance to the value of 50 Ω using two highly-asymmetrical impedance elements are use as match standards. Our experiments showed a very good agreement of the transfer TMR with the benchmark NIST multiline TRL up to 110 GHz (Attachment 13.1).

3.5 Multiport Calibration

Some special device characterization applications require multiport calibration and measurement techniques (e.g. [51]). Also, multiport calibration is used for measurements of differential passives and IC's.

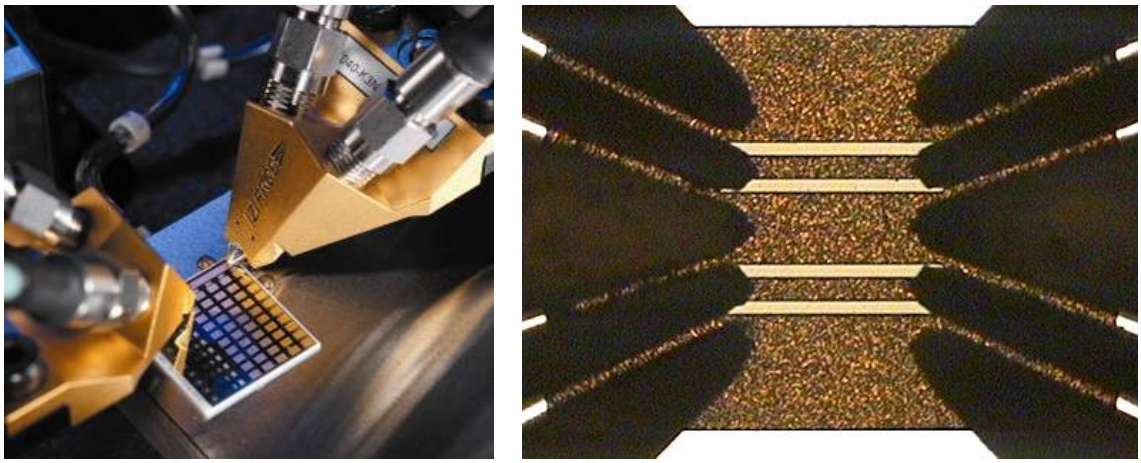
I reviewed multiport calibration theory in [32]. For the *in-situ* calibration, the most promising approach, the RRMT method, integrates the 10-term based algorithm with self-calibration techniques. It was presented for the first time in [52] (Attachment 13.2). My co-author Prof. Holger Heuermann (FH Aachen, Germany) developed the mathematical solution for the generalized RRMT procedure. In this work, I was responsible for collecting measurement data and data analysis. Thanks to Steffen Schott (SUSS MicroTec, Germany) I had access to a 4-port VNA Ballmann S208 built on double-reflectometer architecture. It is important to note, that in 2004, it was the only multiport VNA realizing this advanced architecture.

The RRMT procedure was developed specifically for the probe-tip calibration. The algorithm tolerates the reflection coefficients of the open and short standards. The partly unknown characteristics are calculated from the self-calibration step, based on the two-port transfer TMR (3.17)-(3.33). It is repeated twice: for the short and for the open. The match and thru standards must be fully known.

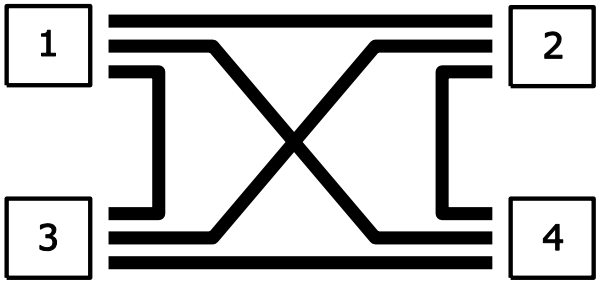
RRMT implemented two TMR self-calibration steps between measurement ports 1-2 and 3-4. The algorithm required all thru standards to be fully known, including the loop-back and cross-over elements (Fig. 3.3). All thru standards were assumed to have a characteristic impedance of 50 Ω and to be lossless. As it was demonstrated in the paper, such simplification was valid for the standards implemented in the multiport CSR-family of calibration substrates. Obviously, this might not be the case for on-wafer scenario or for higher frequencies.

The RRMT calibration was extended to integrate the unknown-thru USMO self-calibration steps from [53]. Now, the USMO self-calibration stet could be used between measurement ports that require the loop-back and the cross-over thru elements (Table 3.2). The concept was proved on the 40 GHz multiport measurement system [54] (Attachment 13.3). For this paper, I planned the entire work, derived the mathematical solution, acquired measurement results, did the calculations and wrote the paper. My two co-authors, Prof. Holger Heuermann (FH Aachen, Germany) and Steffen Schott (SUSS MicroTec, Germany) provided scientific and management supervision respectively.

The new calibration method received the commercial name "generalized RRMT+". It was further implemented in the commercial calibration software SussCal Professional from SUSS MicroTec and is patented under US7768271 [55]. The transfer TMR method was also implemented in SussCal Professional under the commercial name LRM+.



a) b)



c)

Fig. 3.3: Configuration of a 4-port wafer-level calibration: two dual |Z|-Probe (a), example of the straight thru (port 1 – port 2, port 3 – port 4) from the CSR-substrate family (b), loop-back (port 1 – port 3, port 2 – port 4) and cross-over connections (port 1 – port 4, port 2 – port 3), (c).

Table 3.2: Self-Calibration Steps of the Generalized RRMT+ Method

Ports	**1-2**	**3-4**	**1-4**	**2-3**	**2-4**	**1-3**
Self-calibration steps	TMR	TMR	UMSO	UMSO	UMSO	UMSO
Self-calibration product (S-parameters)	Open, Short	Open, Short	Thru	Thru	Thru	Thru

3.6 Conclusion

In this chapter, the key requirements to *in-situ* calibration methods were determined taking into account capabilities and limitations of modern silicon-based processes for fabrication of custom standards. It was also shown that, in this context, the transfer TMR is an appropriate method.

Mathematical solution for the transfer TMR was derived. The capability of this method to use arbitrary and asymmetrical impedance elements was proven using the NIST methodology. For the first time, the accuracy of the TMR was quantitatively verified for the case of application of highly asymmetrical loads. It was proved that the method is comparable with the reference NIST multiline TRL.

Also, the calibration solution RRMT+ was developed as the extension of the transfer TMR for multiport applications. It was demonstrated that the RRMT+ outperforms the reference multiport method and is also suited for *in-situ* implementation. During this work, I was in charge of implementing both calibration methods in the commercial calibration software SussCal Professional.

For further improvement, the error model shall be extended including crosstalk terms into it. It is of particular interest at sub-THz frequencies. While such extension goes beyond the scope of this work, it is important to note that the implementation steps of such calibration methods on a custom test chip will be similar to those discussed in the next chapters.

4 DESIGN OF ON-WAFER CALIBRATION STANDARDS

For implementing the transfer TMR and the multiline TRL methods on the high-performance silicon processes, I initiated a close cooperation with engineering groups from IHP Microelectronics (Germany), IBM Microelectronics (Essex Junction, VT, USA), and STMicroelectronics (Crolles, France). We developed and proved concepts for on-wafer calibration for the bipolar SiGe:C process from IHP (published in [48]), the CMOS 8SF process from IBM (published in [56]), and the BiCMOS9MMW process from STMicroelectronics (published in [57-59]).

For these projects, I framed the design requirements and worked with every engineering group to adopt them to specifics of the selected process. Standards were laid out by in-house designers. IBM and IHP performed in-house measurements. I measured test chips from STMicroelectronics at facilities of Cascade Microtech GmbH (Germany), University of Dresden (TUD CEDIC, Germany), and Ferdinand Braun Institute for High Frequencies (FBH, Berlin, Germany). I performed calibration calculations, analysis of the results, planned all papers and wrote the related sections.

4.1 Design Tradeoff

RF probes and commercial calibration standards are always provided by the same vendor. Therefore, it is the responsibility of the probe vendor to optimize the design of commercial standards and to guarantee accurate probe tip calibration. Electrical characteristics of planar commercial standards ensure that the calibration reference plane is accurately defined and that the calibration reference impedance $Z_{REF} = 50\ \Omega$.

In contrast, customized calibration standards should satisfy significantly more requirements balancing the design tradeoff:

1. The measurement reference place should be located as close as possible to the terminals of the intrinsic DUT. This will allow excluding all backend parasitics from the DUT measurement results;
2. Elementary devices (for example transistors, spiral inductors, etc.) significantly vary in their geometries: short, long, single-finger, multi-finger. There is not only one common reference plane, but one reference plane per geometry;
3. There are three common definitions of the device terminals (location of the measurement reference plane):

   a. Input and output of an intrinsic device. This reference plane is requested by modeling engineers;
   b. A certain location at the top metal level. This reference plane is requested by circuits designers;
   c. At device contact pads (probe tip end). It is a common view of characterization engineers on every device;
4. For both MOS and BiCMOS processes, only the top metal layers are suitable for broadband RF passives, e.g. calibration standards;
5. The lumped load element requires a resistor. Typically, resistors are made from poly-silicon and are located directly on the substrate;

Balancing these requirements, the following design rules for custom calibration standards for silicon processes were stated:

1. Design distributed standards (thru and lines) as well as reflect (both open and short) at the top metal layer;
2. Use poly-silicon for the load resistors. In this case, the equivalent impedance of the load is given by the load resistance and the impedance of via stack (load reactance);
3. Set the calibration reference plane at the top metal level and at a port distance corresponding to the widest intrinsic DUT;
4. When required, move the measurement reference plane to the DUT terminals (metal 1) using an appropriate de-embedding method. The S-parameters of the de-embedding elements should be corrected with respect to the on-wafer calibration, e.g. to the measurement reference plane that is located at the top metal level;
5. Implement additional elements for quantitative verification of the calibration accuracy. As it will be shown later, a serial attenuator can serve as a simple verification element for the transfer TMR. A symmetrical pad open de-embedding element can also be chosen for the qualitative accuracy verification of both TMR and TRL methods (when short element was used as the calibration reflect).

The TMR standards were added on IHP's BiCMOS process test chip. IBM and STMicroelectronics processes allowed implementing both multiline TRL and transfer TMR test chips. The test chip of every process included de-embedding elements. The type of these elements as well as their design were defined according to in-house rules and device characterization methodology applied by each partner.

Next, the most extensive set of calibration and de-embedding elements implemented on STMicroelectronic's BiCMOS9MMW process will be presented. Then, the specifics of custom standards from other processes will be discussed.

4.2 Design of RF Contact Pad and Device Interface

Design rules for RF DUT contact pads have been well established from the very beginning of the wafer-level RF device characterization (e.g. [60-62]). The basic requirement is that the pad configuration should support the Ground-Signal-Ground (GSG) RF probes if the measurement frequency exceeds 10 GHz. The size of an individual pad is subject to optimization under the following criteria:

1. Provide minimal pad parasitic capacitance;
2. Reduce the pad to the minimal possible size to save the on-wafer "real-estate" for devices;
3. Support mechanical capabilities of preferred RF probe technology. The pads should be long enough to keep the probe in contact when it skates forward due to overtravel;
4. Address specifics of contact pad metallization material. The required probe overtravel on Al pads is greater than on soft materials, such as Cu and Au. In result, the probe forward skate is longer, thus the pads should be larger;
5. Allow multiple re-probing of DUT, e.g. for characterization across multiple temperatures.

Considering these five criteria, the RF contact pads are laid out as shown in Fig. 4.1 (b). They support probes with 100 µm pitch and have a probe-to-probe distance of 150 µm. It is the same spacing value as it is used on conventional commercial alumina calibration substrates. It enables an automated measurement and allows calibrating to the probe-tip without probe repositioning.

The BiCMOS9MMW process uses aluminum for pad metallization. Aluminum oxidizes quickly under atmospheric conditions. It builds up an Al_2O_3 layer that is hard to break through. As a result, the probing on Al pads requires the probe overtravel from 25 µm to 75 µm (e.g. [63]) ensuring reliable and repeatable contact. Taking into account positioning accuracy and repeatability of conventional automated probe systems as well as mechanical capabilities of the Infinity Probe technology from Cascade Microtech (the in-house preferred probe design), the pad dimensions are laid out as 100 µm x 85 µm and 40 µm x 85 µm for the ground and the signal pads respectively (see Table 4.1). Additionally, the signal pads are shaped out in an octagon-like form to further reduce the pad parasitic capacitance.

Table 4.1: Contact Pad Design of the BiCMOS9MMW

	Signal, Ground Length	Ground Width	Signal Width	Probe Pith	Signal-to-Ground Gap	Probe Spacing
Parameter, µm	85	100	40	100	25	150

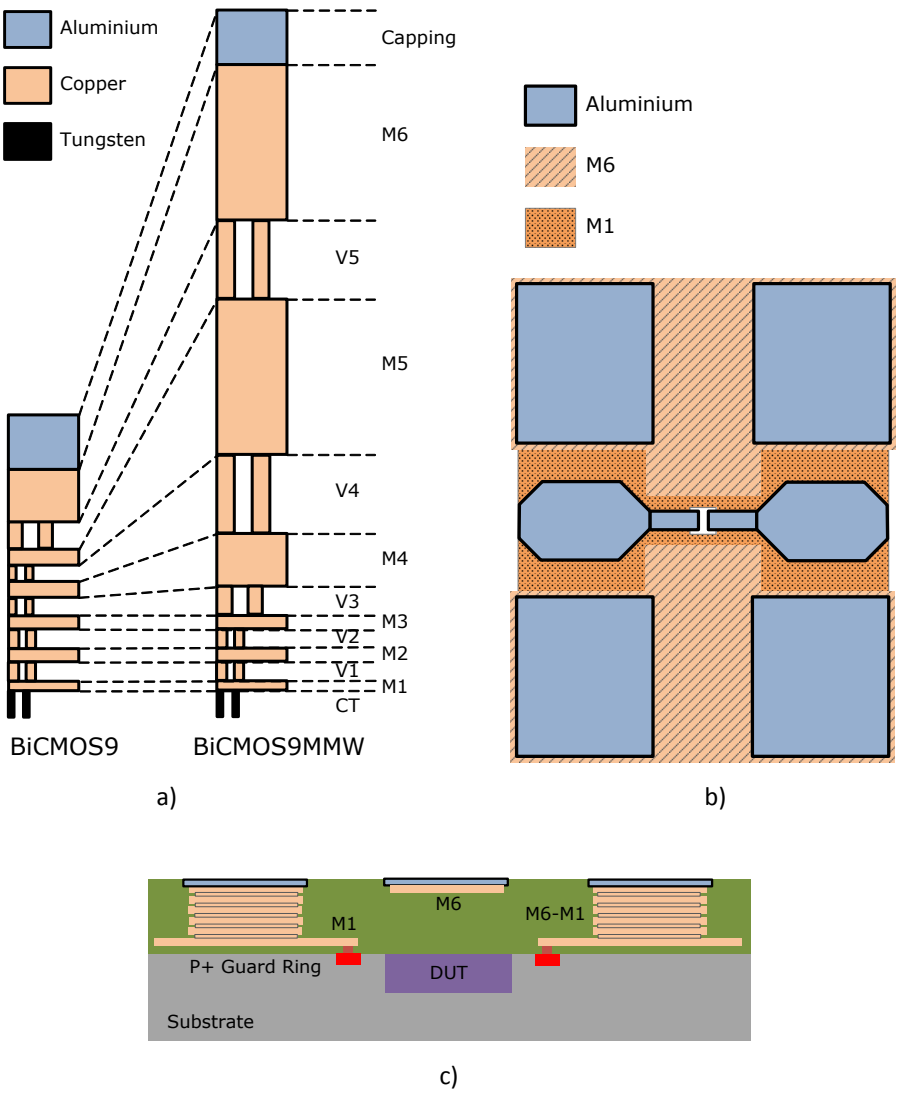


Fig. 4.1: Schematic view of the BEOL cross-section of the BiCMOS9 and BiCMOS9MW technologies (a), the RF contact pad design (b) and the cross-section of the DUT interface (c).

The interface to the device realizes the grounded coplanar design with a metal 1 ground shield and a meshed ground continuously spread over the via stack from the top metal 6 layer (M6) down to metal 1 (M1, Fig. 4.1). The ground plane eliminates the losses caused by the substrate resistivity. Also, it makes the parasitic of the signal pads purely capacitive and facilitates the de-embedding up to high frequencies.

Transistors are laid out in the common collector configuration, i.e. the emitter and the substrate are shorted to the ground preventing high frequencies resonances. In order to reduce substrate effects, all transistors have a P+ guard-ring at a minimum distance of the N-epitaxial well that is connected to the ground shield [58].

4.3 Location of the Reference Plane

As it was already briefly noted above, characterization, modeling, and design engineering communities have different points of view on the "device". The location of the characterization reference plane is still a subject of debate: at the probe tip, at the lateral device terminals or at one of the levels of the BEOL. Up to now, the following procedure has prevailed as the industry's standard:

1. The system is calibrated to the probe tip end by the SOLT method;
2. The BEOL parasitics are de-embedded using the open and short contact pad dummy elements [8];
3. The device RF Figures of Merits (FoM) are extracted at relatively low frequencies (typically at 20 GHz);

Device characterization engineers favor calibration of the measurement system to the probe tip end using commercially available alumina calibration substrate (Fig. 4.2). Dealing with optimized and characterized by vendor calibration standards simplifies the task of system calibration. It also allows quick verification of the calibration accuracy with the help of additional reference elements available from the calibration substrate. Still, this approach may lead to a serious over- or under-estimation of FoM of sub-THz f_T /f_{MAX} HBTs [64].

Design engineers prefer SPICE models that include a minimum of BEOL parasitics and allow realistic pre-layout simulations (schematic mode). Advanced transistors showing very high f_T/f_{MAX}, have junction capacitances of merely several femto Farads. Here, any small parasitics may strongly affect transistor's FoM. Therefore, the top-metal location (e.g. M6, Fig. 4.2) is preferred. For designers, it is important that the Process Design Kit (PDK) includes such SPICE libraries.

In contrast, modeling engineers aim to extract "physics-based" parameters of the device compact models. Therefore, the reference plane has to be shifted as close as possible to the intrinsic device terminals (e.g. M1, Fig. 4.2). The requirements for device modeling are more challenging.

Designing *in-situ* broadband transmission lines (a crucial standard for the TRL and the TMR calibrations) close to the DUT terminals (e.g. M1 or M2 levels) is problematic for silicon processes. The first metal layers are not suitable for mm-wave passives. A more reasonable approach is using the top metal level (M6 for the BiCMOS9MMW, Fig. 4.1) that facilitates good RF performance of the line [65]. Therefore, the optimal position of the *in-situ* calibration plane is at the top metal level M6.

If required, the on-wafer calibration reference plane can be shifted from the M6 to the M1 level by a conventional de-embedding approach. Because the parasitic impedance of the contact pads and interconnect lines are already calibrated out (included into the systematic measurement error model), the equivalent impedance of the de-embedding elements should represent the parasitic impedance of the M5-M1 via stack, that is mostly of pure lumped nature. Measurement results later proved this statement (see Chapter 7).

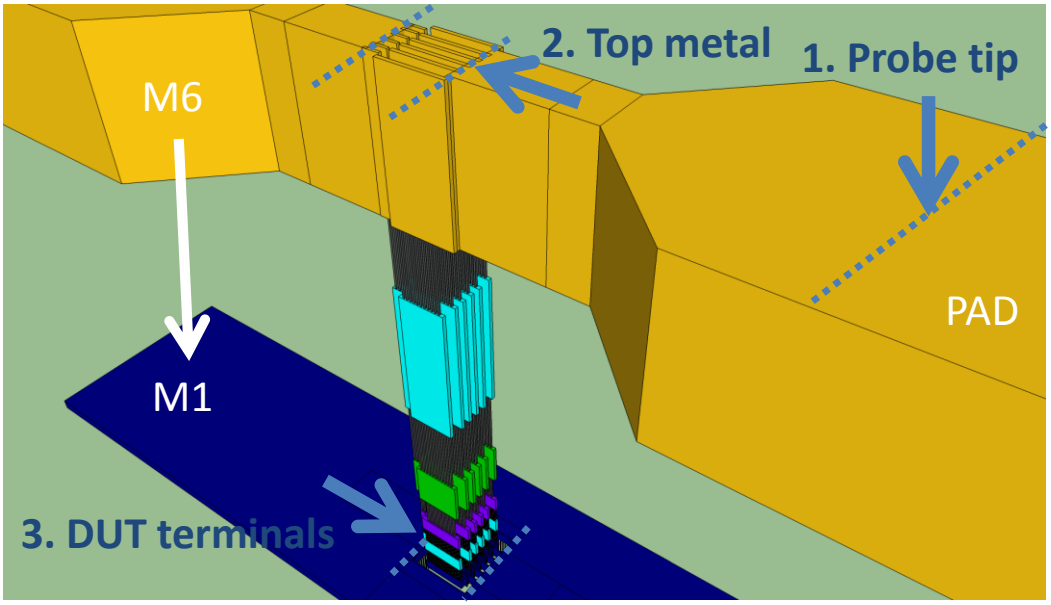


Fig. 4.2: Three different locations of the reference plane: probe tip, top metal, DUT terminals for a complete open dummy. Example for the CBEBC HBT.

For the probe-tip calibration, the de-embedding elements should capture the equivalent impedances of the contact pads and the entire DUT BEOL parasitics. Thus, the reference plane can be moved from the probe tip to the top metal M6 level or to the intrinsic DUT terminals at the M1 level (Table 4.2). This is challenging especially for small device geometries and at frequencies above 40 GHz [39].

Table 4.2: Location of the Reference Plane

Calibration	Probe Tip	Top Metal	DUT Terminals
Probe tip	Straight	De-embedding of contact pad interconnect line parasitics	De-embedding of the entire DUT infrastructure
On-wafer	N/A	Straight	De-embedding of M6-M1 parasitics

4.4 Calibration Standards

A full set of standards was laid out addressing requirements for the multiline TRL and the transfer TMR calibration methods (Fig. 4.3). Additional elements were placed on the test chip as well (e.g. a symmetrical attenuator).

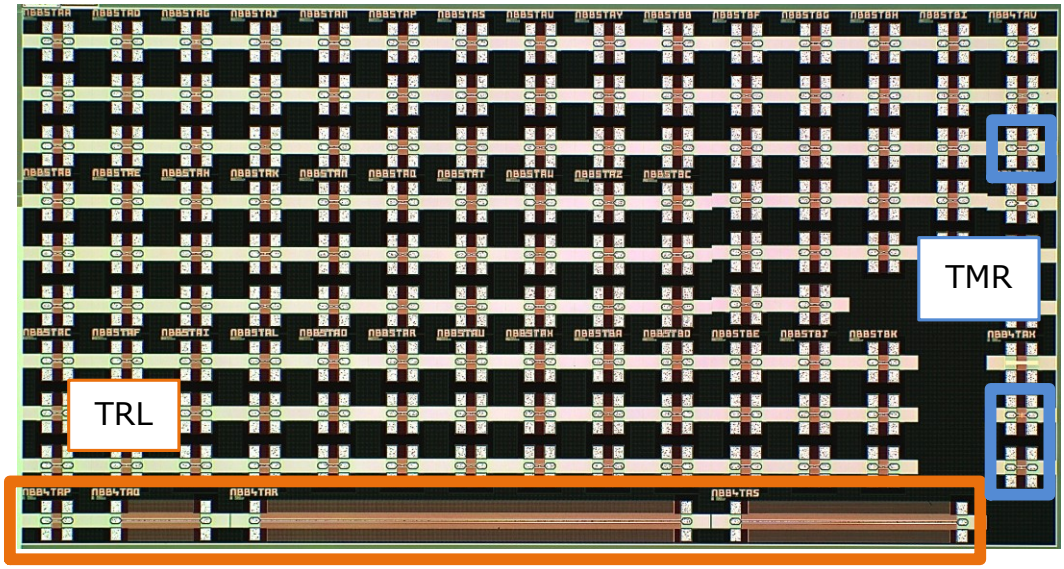


Fig. 4.3: Test chip of the STMicroelectronics' Si/SiGe:C BiCMOS9MMW process technology. The test chip includes the transfer TMR and the multiline TRL calibration standards. Reproduced with permission of STMicroelectronics.

4.4.1 Thru and Line

The thru and the line standards are designed as $Z_{LINE} = 50\ \Omega$ M1-shielded grounded coplanar waveguides with a signal width of about 10 µm and a gap to the grounds of about 9.5 µm (Fig. 4.4). The implementation of the M1 shield minimizes the field penetration to the substrate and reduces the line conductance per unit length.

The effective length of standards is: 51 µm, 549 µm, 1545 µm, and 3039 µm (Table 3.1). It is optimized to cover the frequency range from 1 GHz to 110 GHz. The effective length of standards is found with the help of the approach presented in [66] and realized in Findlen[3].

The ideal TRL calibration conditions are provided when the effective phase delay for a selected pair of lines is 90°. Consequently, the multiline TRL is ill-conditioned if the phase delay is 0°. The effective phase delay for the designed calibration kit is in a range from 60° to 90° for frequencies from 10 GHz to 110 GHz and thus ensures reliable calibration results (Fig. 4.5, left).

[3] A program available from NIST, Bolder CO, USA

Table 4.3: The Length of the Line Standards Embedded on the BiCMOS9MMW Chip

Standard	Design Length, µm	Equivalent Length, µm
Thru	51	0
Line 1	549	499
Line 2	1545	1494
Line 3	3039	2988

For optimized conditions, the standard deviation parameter calculated by NIST Mutical program should not exceed the value of 1 across the frequency range of interest. Fig. 4.5 (right) shows the standard deviation calculated for the designed calibration kit and proves that it meets this requirement from 10 GHz to 110 GHz.

Taking into account the results for the effective phase delay and standard deviations, the multiline TRL can be further considered as accurate reference calibration for the frequency range from 10 GHz to 110 GHz.

After analysis of device geometry variations (short one-finger and long multi-finger transistor from the BiCMOS9MMW design kit), we decided to set *in-situ* calibration reference plane to 7 µm away from the center of the thru. This requirement was considered when designing the reflect (short) and the match (load) standards.

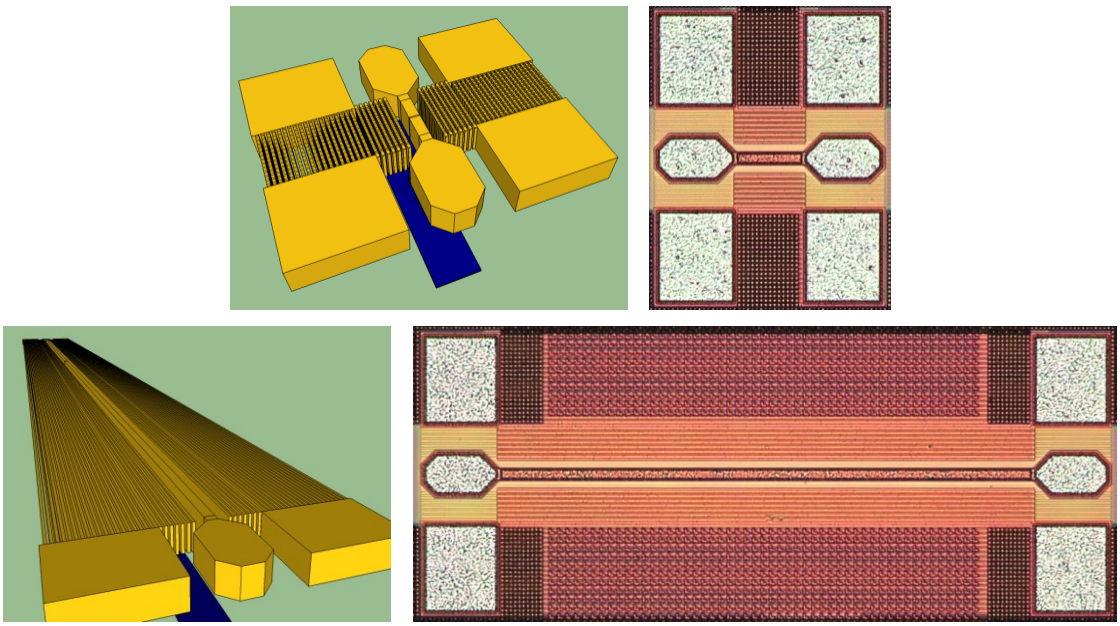


Fig. 4.4: 3D schematic view and a photograph of the thru (top) and line (bottom) calibration standards.

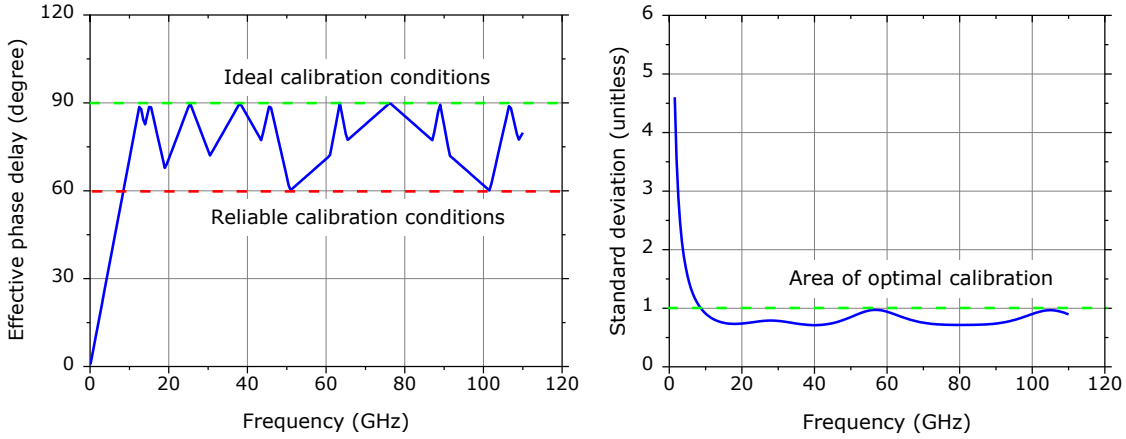


Fig. 4.5: The effective phase delay (left) and the multiline TRL standard deviation (right) calculated for the designed calibration kit.

4.4.2 Short

The high-reflective symmetrical reflect standard is designed as two shorting bars located 7 µm away from the center of the thru standard (Fig. 4.6). This is the only difference to the thru standard.

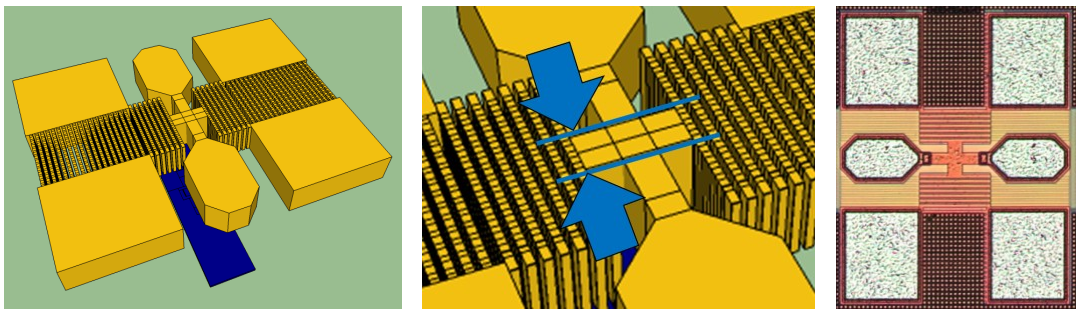


Fig. 4.6: 3D schematic view, a zoomed view and a photograph of the short standard.

The S_{11}, and S_{21} parameters are shown in Fig. 4.7. The results are measured with respect to the on-wafer (M6) multiline TRL and compared against the probe-tip (ISS) short standard. The custom short is less reactive. As expected, the port-to-port crosstalk is about 15 dB higher compared to the short from the ISS. The *in-situ* shorts are much tighter to each other with only 14 µm distance (vs. 150 µm distance for the ISS short). The crosstalk for the *in-situ* short is less than -20 dB within the entire frequency range of interest. The element provides sufficient port isolation and is suitable for a reliable calibration.

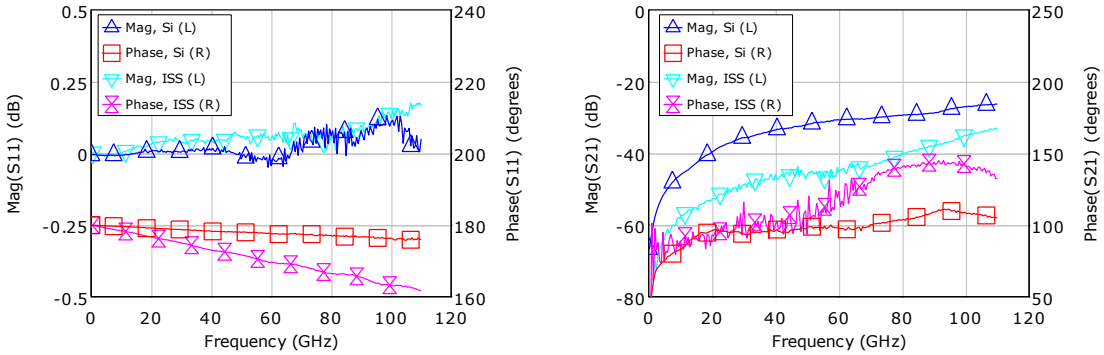


Fig. 4.7: S_{11} and S_{21} parameters of commercial and custom short (reflect) standards measured with respect to the multiline TRL for both probe tip and on-wafer calibration.

It is interesting to note that the crosstalk for the custom short has almost purely capacitive behavior, whereas the ISS short shows a complex crosstalk nature above 50 GHz.

The magnitude of the S_{11} shows a similar pattern for both *in-situ* and ISS elements: it continuously increases with the frequency up to 0.2 dB at 110 GHz for the ISS short. The custom short repeats this effect from 60 GHz. I attributed this effect to the calibration residual error caused by the probe tip design. The maximum error of 0.2 dB at 110 GHz can be neglected for now. I will come back to the probe dependent calibration residual error in Chapter 9.

4.4.3 Load

The load is a single (per port) 50 Ω N+ salicided poly resistor located close to the M1 level (Fig. 4.8). The resistors are laid out symmetrically for both ports. Often engineers repeat the layout of a probe-tip load with two 100 Ω resistors connected in parallel for the custom load standard, see Fig. 4.9, [67, 68]. The only advantage of such layout is that it reduces the space taken by the standard on the substrate. So, the commercial vendors can put more loads on the substrate increasing its lifespan and reducing the cost of RF calibration.

The fabrication process inaccuracy may lead to a high in-port asymmetry between the two 100 Ω resistors. The equivalent resistance of the load will be misbalanced. To solve this problem for commercial alumina standards, the resistors are trimmed to the specified values during the manufacturing process. In contrary, trimming *in-situ* resistors is very difficult, impractical and often not possible at all. That is why, it is highly recommended to use one resistor per port, as shown in Fig. 4.9 (right).

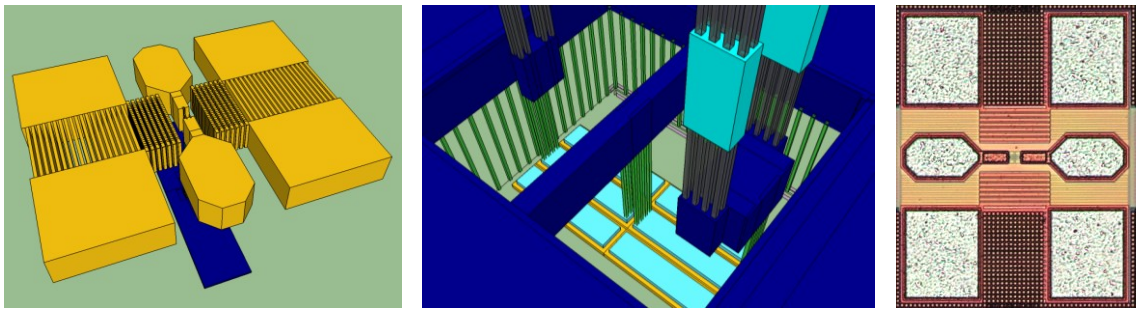


Fig. 4.8: 3D schematic view (let), a zoomed view (middle) and a photograph (right) of the load standard.

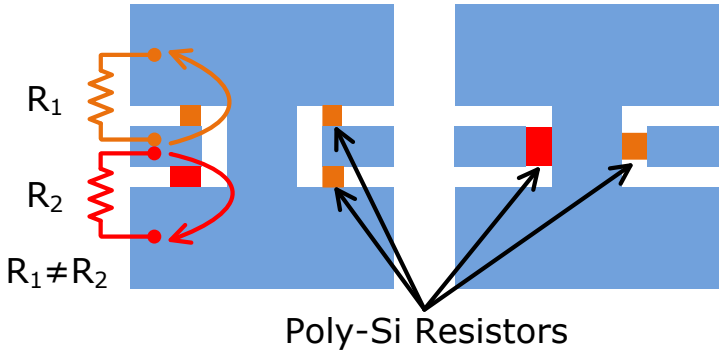


Fig. 4.9: Schematic of the load: not-recommended (left) and recommended (right) design of the 50 Ω resistor for a custom match standard. The port 1 resistor of the first load is unbalanced due to fabrication inaccuracy.

The via stack repeats the shortest single-finger transistor (Fig. 4.8, middle). Therefore, the load reactance is slightly asymmetrical between ports. However, it can be accurately handled by the transfer TMR calibration capability, as it was shown in Chapter 3 and in [48, 50].

4.5 De-Embedding Elements

The modeling test chip of the STMicroelectronics' BiCMOSMMW9 process includes an extensive set of de-embedding elements. The in-house de-embedding strategy is built on the proprietary scalable six-step method (Fig. 2.11). The method requires the following dummy elements: probe short, pad open, pad short, thru, device open and device short. In addition, the complete open and the complete short elements are included. These elements are specific per device geometry, as we discussed in [59].

4.5.1 Pad Open and Pad Short

The pad open and the pad short de-embedding elements are laid out to represent the serial and the parallel parasitic impedances of the pad at the M6 level. The pad open keeps the signal pads (drawn at the top metal only) and the ground pads (Fig. 4.10). The signal pad includes a few micrometers of the signal line (launch stab). It takes into account the pad-to-line discontinuity and provides well-defined signal launching from the pad into the transmission line of the thru de-embedding element. The length of the launch stab is kept the same across all de-embedding elements. All interconnect metal levels except M6 and the via stack are removed.

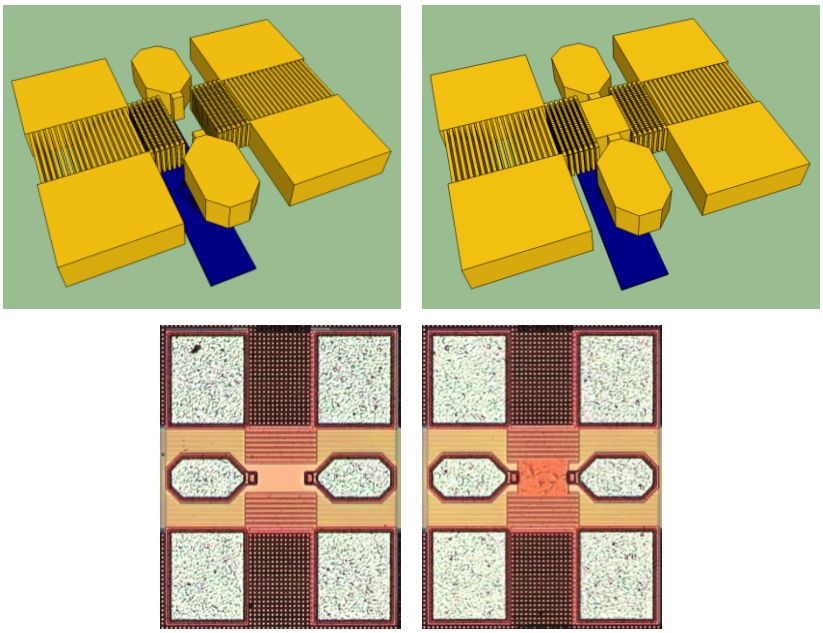


Fig. 4.10: 3D schematic view (top) and a photograph (bottom) of the pad open (left) and the pad short (right) elements.

The pad short has a top metal shorting area between the extremity of the pads and the closest ground metal stack. The via stack between M6 and M1 is kept and all M1 terminals are shortened over the DUT, while the DUT itself is removed.

4.5.2 Probe Short

The design of the probe short resembles the pad open, but the signal pads are shorted to the ground by the large M6 ground plate (Fig. 4.11). As mentioned in [39], there are two purpose of this element. First, it evaluates any discrepancies of the probe-tip calibration. Secondly, it ensures the coherence of the RF/DC resistance measurements.

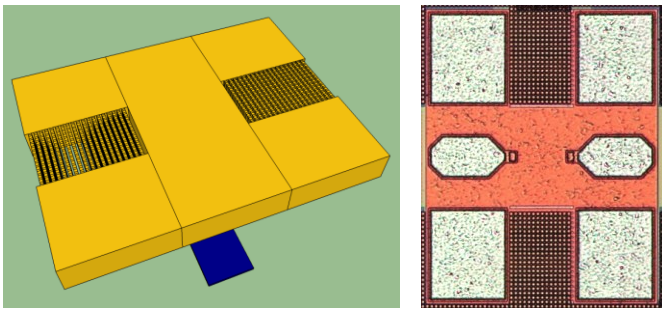


Fig. 4.11: 3D schematic view and a photograph of the probe short elements.

4.5.3 Complete Open and Complete Short

To move the reference plane to the intrinsic DUT terminals, the dummy elements must repeat the geometry of each transistor. Therefore, the complete open should replicate each DUT element. While excluding the contact vias, it includes all metals and the via stack between the end of the top layer line and the first metal above the DUT (Fig. 4.12).

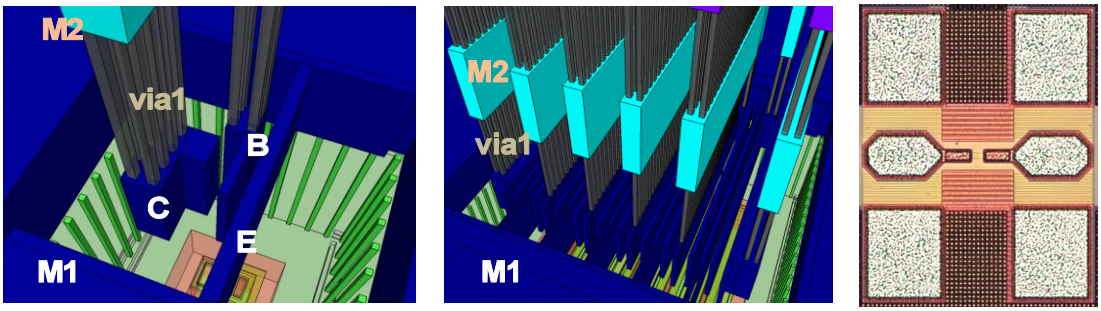


Fig. 4.12: 3D zoomed-in view of the M1 and M2 area 3D schematic of the complete open element designed for a short single-finger (left) and a long multi-finger (middle) DUTs, as well as its photograph (right).

Obviously, the equivalent capacitance of the complete open element depends on the DUT type. However, it is always greater than the equivalent capacitance of the pad open, as it also includes a parasitic capacitance between M6 and M1 layers. A comparison for S_{11} and the port 1 equivalent capacitance C_1 of the complete open element is given in Fig. 4.13 for the DUT in CBEBC configuration with W_E=0.23 µm and L_E=0.15 µm vs. the pad open.

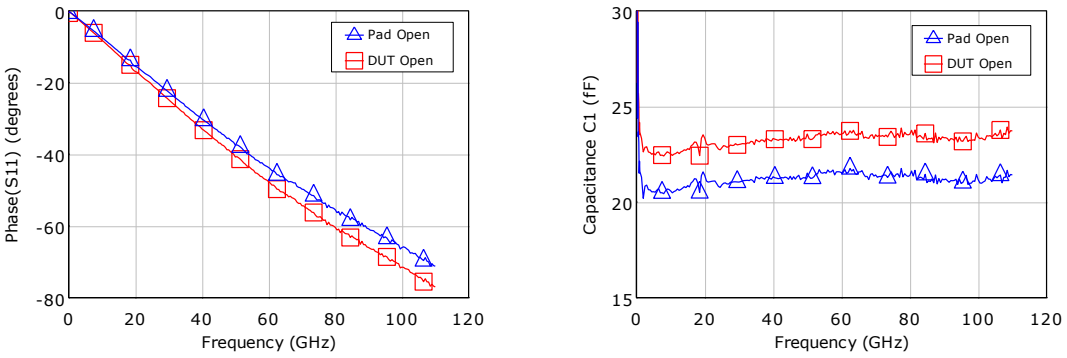


Fig. 4.13: Comparison for the phase of S_{11} (left) and the equivalent capacitance C_1 for the complete open and the pad open elements measured with respect to the probe-tip multiline TRL calibration.

Similar to the complete open, the complete short design depends on the DUT type. It is drawn from the DUT test structure where the device is removed and the access to the transistor pins is shorten over the M1 plate (Fig. 4.14).

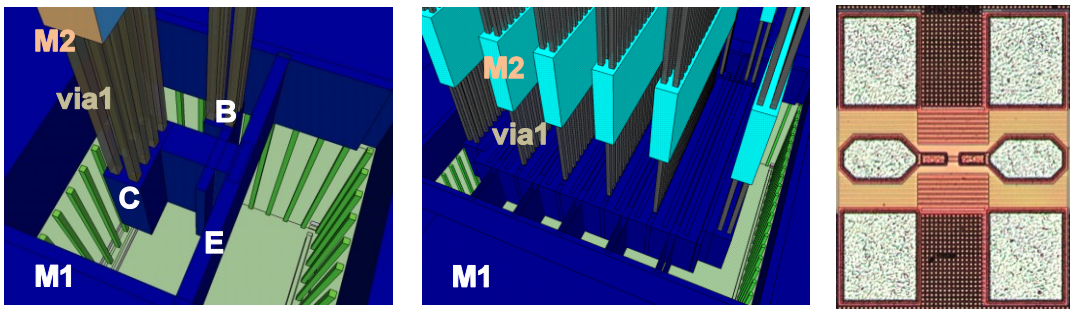


Fig. 4.14: 3D zoomed-in view of the M1 and M2 area of a complete short element designed for a short single-finger (left) and a long multi-finger (middle) DUTs, as well as a photograph (right).

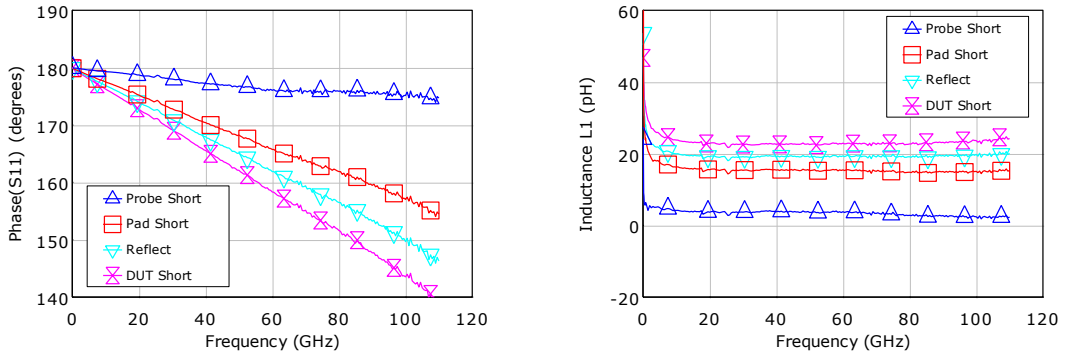


Fig. 4.15: Comparison for the phase of S_{11} (left) and the equivalent inductance L_1 for complete short, probe short, pad short, and reflect elements measured with respect to the probe-tip multiline TRL calibration.

Again, the equivalent inductance of the complete short depends on its layout. It is always greater than the equivalent inductance of the probe short, pad short and reflect elements, as it includes the M6-M1 via stack parasitic inductance. For example, Fig. 4.15 compares the S_{11} parameter and the port 1 equivalent inductance L_1 of the complete short for the DUT in CBEBC configuration with W_E=0.23 µm and L_E=0.15 µm vs. the probe short, pad short and the reflect measured and extracted with the respect to the probe tip multiline TRL.

Both Fig. 4.13 and Fig. 4.15 impressively show that the BEOL parasitics increase the closer we get to the terminals of the intrinsic device.

4.6 Calibration Standards and De-Embedding Elements Implemented in the IHP BiCMOS SiGe:C Process

The first implementation of the transfer TMR method was done on the IHP BiCMOS SiGe:C process (Fig. 4.16). The modeling chip included thru, load, and short calibration standards (Fig. 4.17).

At the time of the experiment, the IHP in-house de-embedding strategy was based on the three-step method. The method uses open, open-short, short-open, and thru dummy elements (Fig. 4.18). The calibration standards and the dummies were designed such that the thru standard could also serve for the benchmark de-embedding step. It saved one slot on the test chip were we put the symmetrical attenuator for purpose of calibration and de-embedding accuracy verification.

Other technical details of the standard design are proprietary information of IHP Microelectronics and cannot be published here.

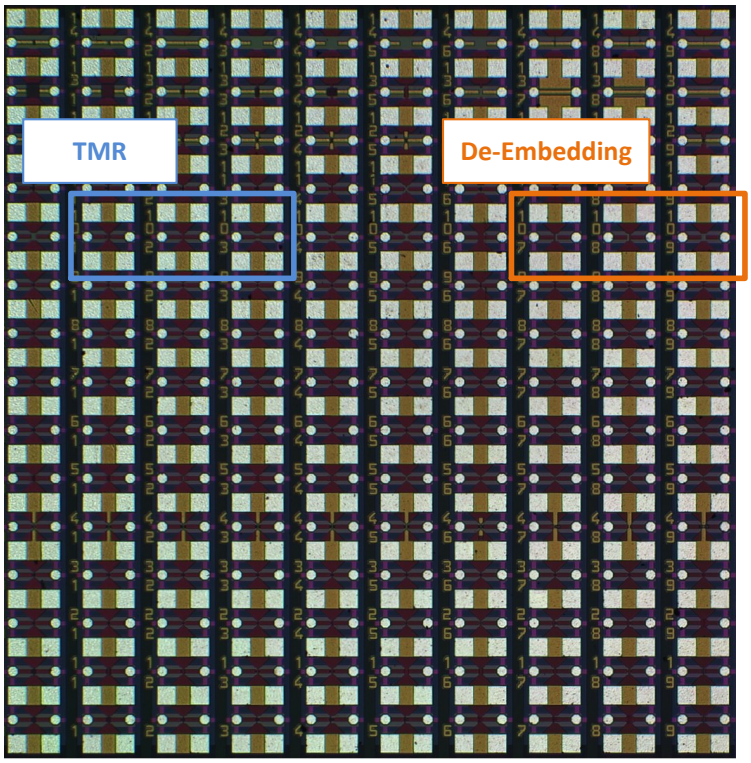


Fig. 4.16: Test chip of the IHP SiGe:C BiCMOS process with transfer TMR standards and the three-step de-embedding dummy elements. Reproduced with permission of IHP Microelectronics.

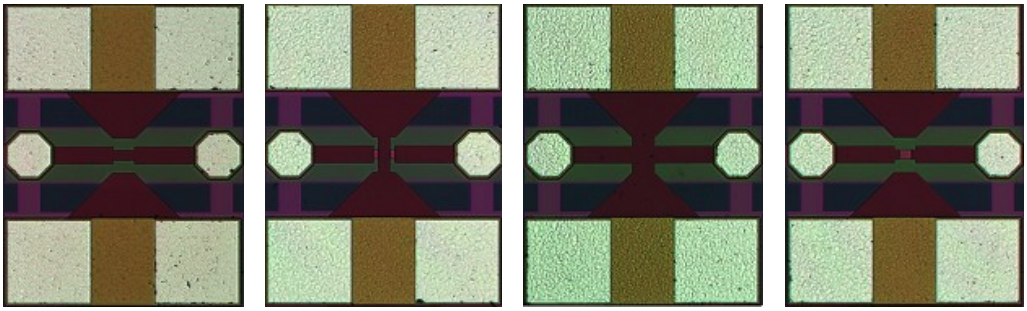


Fig. 4.17: Transfer TMR calibration standards from the IHP SiGe:C precess, from left to right: thru, load, short, and the verification element attenuator.

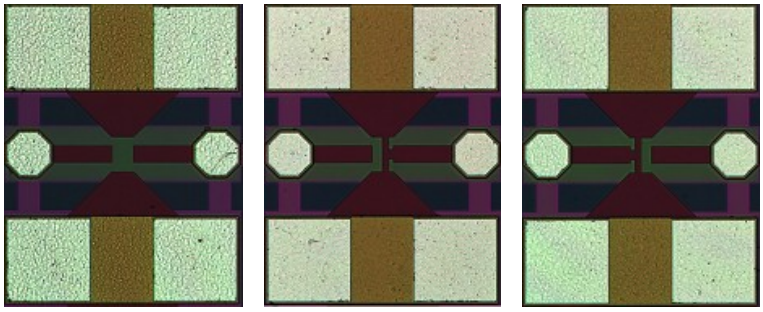


Fig. 4.18: Three-step de-embedding dummy elements from the IHP SiGe:C process test chip. From left to right: open, open-short, and short-open.

4.7 Calibration Standards Implemented in IBM RF CMOS 8SF Process

We implemented the multiline TRL as well as the transfer TMR standards on the IBM advanced RF CMOS 8SF 0.13 µm process. The calibration set included thru, three lines, open, short, and load.

Standards were fabricated within a typical 2-port GSG on-wafer probe pad set with aluminum metallization. The ground pads, signal pad, and signal launch lines were placed on an upper metal level layer, while a meshed ground plane was placed under the signal geometries on the first metal level layer. The transmission lines were laid out as extensions of the signal launch lines. The thru and line signal connector was placed one level below the pads and was made of copper. The thru length was 100 µm and the width 18 µm. The length of lines was optimized for the frequency range of 1 GHz to 110 GHz. The ground plane was placed on the first metal level. The space between bottom of signal line and the top of ground was 8.4 µm. The CPW grounds are 45 µm wide. The gap between the edge of signal and the edge of ground was 68.5 µm. Such design ensures the main microstrip mode is the dominant line propagation mode in the frequency band of interest.

The signal contact pad measured 45 µm x 75 µm, while we used 95 µm x 75 µm ground pads. A photograph of the thru standard is shown in Fig. 4.19.

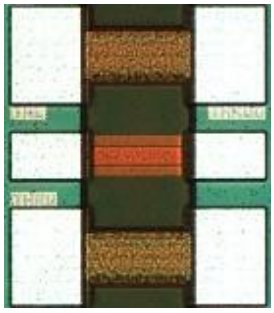


Fig. 4.19: The thru standard implemented in IBM RF CMOS 8SF process test chip. Reproduced with permission of IBM Microelectronics.

The de-embedding elements were designed for the general 4-port method as described in [38]. Besides conventional open and shot elements, the test chip also included open-resistor, resistor-open, short-resistor, and resistor-short. We used the same thru element for both de-embedding and calibration.

Other technical details of the standard and de-embedding element design are proprietary information of IBM and cannot be disclosed here.

5 ELECTRICAL PROPERTIES OF CUSTOM STANDARDS

5.1 Multiline TRL and Transfer TMR Requirements

The key difference between calibration and de-embedding is the "view" on calibration standards and de-embedding elements. In a conventional de-embedding approach, the electrical characteristics of de-embedding elements remain unknown. The only assumption is that a single element represents a part of the pad and interconnects parasitic impedance. So, the parasitic impedance can be measured straightforward and further subtracted from the DUT results.

The calibration approach assumes that the measurement errors (e.g. the parasitic impedances) are captured by a specific error model. The complexity of parasitic impedance equivalent circuit is irrelevant. However, calibration requires a set of standards with known electrical characteristics. Manufactures of commercial calibration substrates meet these requirements as follows [69, 70]:

1. The characteristic impedance of the line is kept within a defined specification and has a nominal value of $Z_{LINE} = 50\ \Omega$;
2. The conductive loss of the line is negligible;
3. The thin film resistor of the load standards is accurately trimmed to $R_{LOAD} = 50\ \Omega$ with accuracy better than 0.3%;
4. The reflection standards (open, short, and load) are optimized for minimal parasitic reactance for a given probe pitch. The equivalent parasitic reactance of a standard is specified (calculated or/and measured) for each probe pitch.

Obviously, these requirements are hard to address for custom standards. As a result, the first attempts to implement custom calibration process for silicon process failed [71].

As it was already discussed in Chapters 2 and Chapter 3, the multiline TRL and the transfer TMR require to know:

1. The characteristic impedance Z_{LINE} of the thru (line) for both TRL and TMR calibration;
2. Impedance of the load Z_{LOAD} for TMR calibration.

5.2 Measurement of the Characteristic Impedance of the Line

Following an extensive research, three techniques were selected to measure the characteristic impedance Z_{LINE} of the line for the IBM CMOS and STMicroelectronics BiCMOS processes:

1. Calibration comparison method from Arz [72];
2. Lumped load method from Williams [73];
3. Electromagnetic simulation.

The objective of my experiments was to achieve reliable results up to 110 GHz. Other methods required an initial probe-tip calibration followed by various pad de-embedding techniques [74-76]. They demonstrated insufficient extraction accuracy at frequencies above 20 GHz or they are cumbersome and less practical. Therefore, I left them out of the scope of this investigation.

The key work on this topic was done together with Phil Corson and Susan Sweeney from IBM Microelectronics (Essex Junction, VT, USA) and Uwe Arz from PTB (Braunschweig, Germany) and verified on the IBM advanced RF CMOS 8SF process. The results were presented in [77] (Attachment 14.1). I developed the entire verification methodology, did all calculations (except extraction of the DUT parameters), and wrote the major part of the conference paper. The design of the custom calibration standards, the electromagnetic simulations and the acquisition of measurement data were done by IBM engineers. The analysis of the results was done together with all co-authors.

For the first time, it was demonstrated that the calibration comparison method from [72, 78] can successfully be used for extraction of the characteristic impedance Z_{LINE} of the *in-situ* calibration lines. However, a well-defined reference calibration is required. Both NIST GaAs reference material RM8130 and the commercial calibration substrate CS-5 (from GGB Industries) were verified for establishing the reference calibration up to 110 GHz.

A strong impact of the probe-tip design and un-optimized reference calibration boundary conditions on the experimental results was found at mm-wave frequencies. This topic will be discussed later in Chapter 9.

It was proven that the lumped load method from [73] can be applied to measure Z_{LINE} of the tested lines from IBM's RF CMOS 8SF process test chip. Later, I verified the lumped load method for BiCMOSMMW9 test chip from STMicroelectronics, [57]. The lumped load method showed results comparable with the benchmark calibration comparison method. The lumped load method is the favorite choice for practical applications. However, it requires that the conductive loss of the line is minimized by special measures of the line design such that it can be neglected.

It remained challenging to achieve a sufficient level of simulation accuracy for custom standards realized in advanced multi-layer technologies.

On-the-fly measurement of some electrical parameters of standards may be needed because they vary from chip to chip, wafer to wafer, and lot to lot due to instability of the fabrication process. This problem is analyzed in Chapter 8.

5.3 Establishing the Reference for the Calibration Comparison Method

One important topic remained behind the scenes in [77]: how to measure and how to verify the characteristic impedance of CPW lines for a commercial calibration substrate at mm-wave frequencies. Previously, the well-defined NIST GaAs reference material RM8130 was used to establish a reference calibration for the calibration comparison method (see e.g. [79, 80]). However, the RM8130 is specified for use up to 40 GHz [81]. To the best of my knowledge, a solid metrological reference for wafer-level measurements above 40 GHz is still missing.

Though RF probe vendors recommend commercial calibration substrates for the probe tip calibration up to sub-THz frequencies, the reference impedance Z_{REF} of such calibration is questionable and, in a more general term, undefined, because:

1. The characteristic impedance Z_{LINE} of the CPW line can significantly differ from its nominal value of $Z_{LINE} = 50\ \Omega$ due to inaccuracies and instability of the fabrication process. Nevertheless, none of the commercial suppliers specifies it for a particular substrate;
2. The interpretation of the reference impedance of lumped-standard based calibration methods (such as SOLT, conventional LRM or LRRM) becomes difficult at mm-wave frequency range. That is why these methods cannot be considered as good candidates for the reference calibration.

To overcome these problems, the following strategy was developed:

1. Measure Z_{LINE} of CPW line from several commercial alumina calibration substrates and verified the measurement method up to 110 GHz;
2. Use the multiline TRL for the reference calibration on alumina substrate;
3. Transfer reference impedance of the multiple TRL to $Z_{REF} = 50\ \Omega$.

It was executed as following. First, the lumped load method was applied extracted the characteristic impedance Z_{LINE} was extracted for three commercial calibration substrates: ISS 101-190 from Cascade Microtech, CSR-3, and CSR-8 from SUSS MicroTec. Next, the accuracy of the multiline TRL performed with and without correction for the line Z_{LINE} was verified against the NIST RM8130. Results proved that the lumped load method delivers a sufficient level of accuracy for alumina substrates. Taking into account that the commercial CPW lines implemented on ceramic exhibit negligible conductive loss, it was assumed that the extracted Z_{LINE} is valid (at least) up to 110 GHz. Therefore the reference multiline TRL calibration can be executed at every commercial alumina substrate.

The results of this work were published in [23] and are co-authored by Ralf Doerner (FBH, Germany) and Steffen Thies (Rosenberger, Germany) (Attachment 14.2). For this paper, I developed the verification methodology, planned the work, defined the measurement campaign, and wrote the conference paper. The measurement results were acquired by Ralf Doerner at FBH facility. I did calculations and the data analysis together with Ralf Doerner.

Later, when working on paper [77], an extensive analysis of two CS-5 calibration substrates from GGB Industries was performed proving the earlier developed approach for measurement of the line Z_{LINE} of commercial alumina substrates.

5.3.1 NIST GaAs Reference Material RM8130

The RM8130[4] consists of a coplanar wave guide multiline TRL calibration set: a 550 µm long thru line, five lines with lengths of 2685 µm, 3750 µm, 7115 µm, 20245 µm, and 40550 µm, and two offset shorts located at a distance of 225 µm from the beginning of the line. Additionally, there are 12 verification reference elements (Fig. 5.1 and Fig. 5.2). The calibration set is fabricated on a GaAs wafer and is fixed on a quartz holder for better handling.

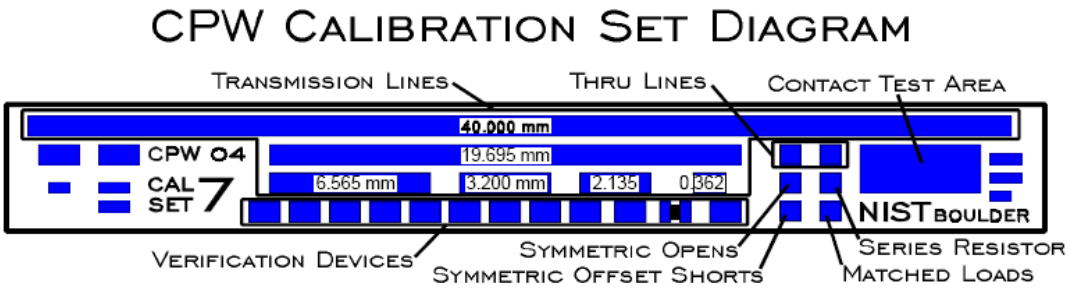


Fig. 5.1: The layout of the NIST coplanar waveguide RM8130. Picture from [81].

The line capacitance per unit length C' of RM8130 CPW is specified according to the individual tests provided by NIST for each reference material. This value is used by the benchmark multiline TRL calibration for the accurate definition of the characteristic impedance Z_{LINE} of the RM8130 lines by (2.25) and the transformation of the measurement system reference impedance to $Z_{REF} = 50\ \Omega$ using (2.51).

Table 5.1 shows the configuration of two setups that I used in experiments from [50, 77]. The setup A at IBM and the setup B at FBH used the same Agilent 8510XF 110 GHz VNA, but were equipped with different RF probes. Also, each laboratory had its own RM8130. That gave the opportunity to compare the electrical characteristics of the CPW lines from two RM8130 and being measured by two probe types.

[4] Available from NIST, Boulder, CO, USA.

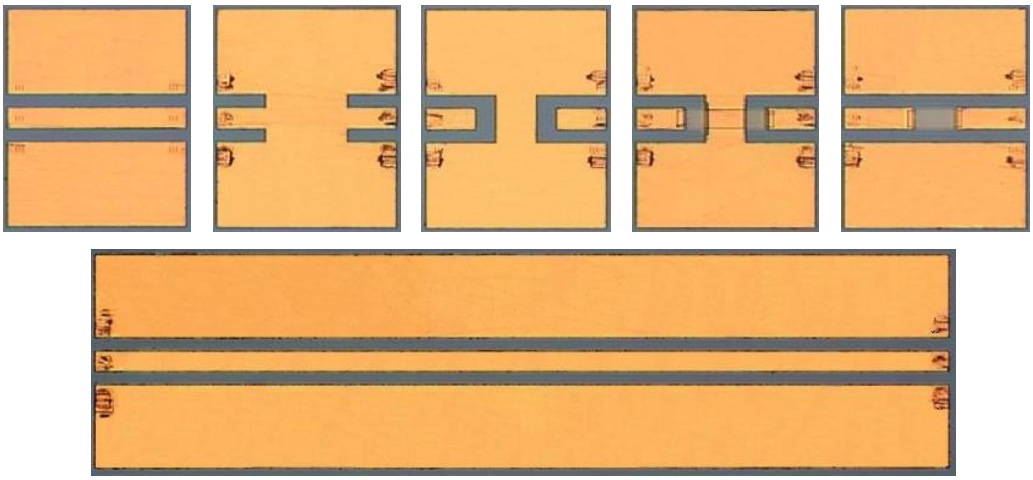


Fig. 5.2: Photographs of some calibation and verification elements implements on the RM8130 CPW, from left tpo right: thu, short, open, resistor, series attenuator, and 2.135 mm line.

Table 5.1: Experimental Conditions

	VNA	RM8130	RM8130 C', pF/cm	Wafer Probes	Test CPW	CPW C', pF/cm
Setup A, IBM	8510XF (Agilent)	#11/4	1.7877	Picoprobe 110 GHz, GSG, 100 µm pitch	CS-5 (a)	1.629
Setup B, FBH	8510XF (Agilent)	#7/3	1.7877	ACP 110 GHz, GSG, 100 µm pitch	CS-5 (b)	1.522

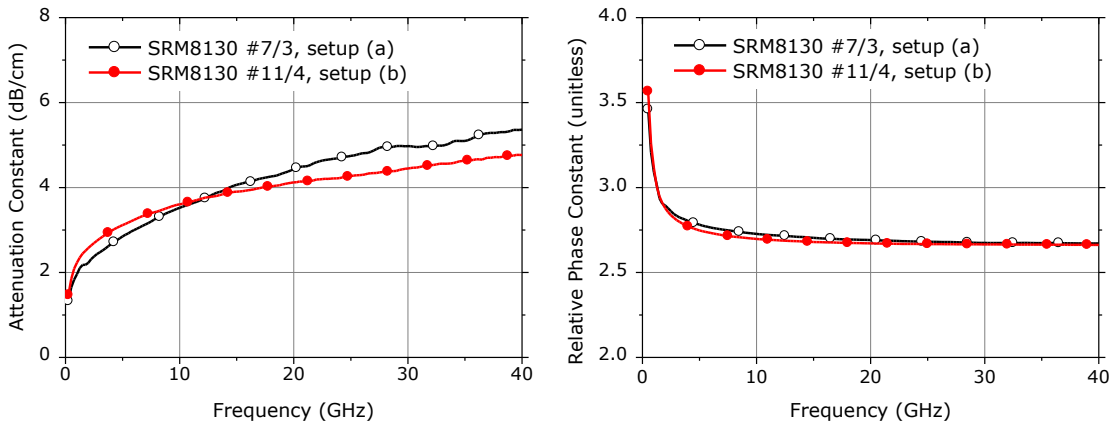


Fig. 5.3: Attenuation constant (left) and the relative phase constant (right) of two RM8130 used in the experiments.

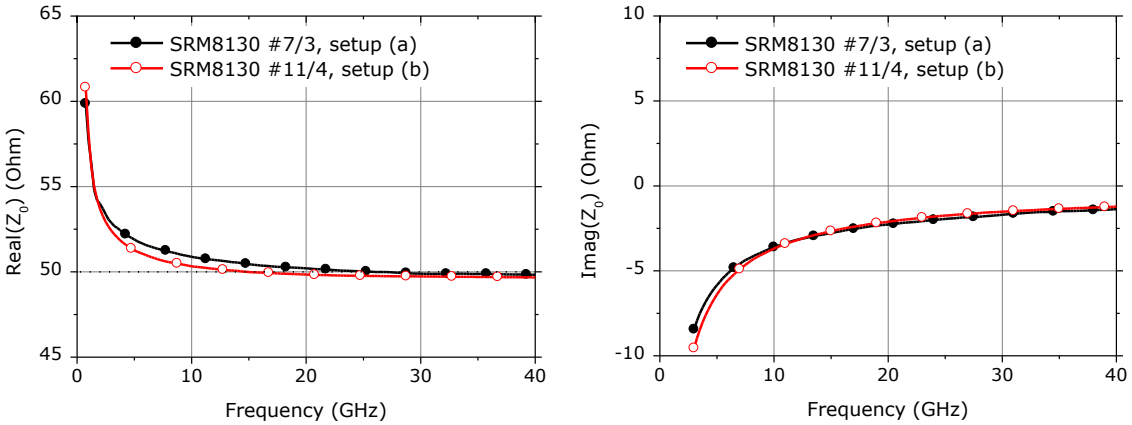


Fig. 5.4: The real (left) and the imaginary (right) parts of the characteristic impedance Z_0 of two RM8130 used in the experiments.

Fig. 5.3 shows the measured attenuation and the relative phase constants of the line for both RM8130 substrates. There is a noticeable difference in attenuation constant while the difference in the relative phase constant is negligible. It was attributed to the impact of the RF probe design and was taken into account for further analysis of the measured data. The characteristic impedance shows comparable behavior for both setups (Fig. 5.4).

5.3.2 Commercial Alumina Substrate as the Reference

Next, the capability of the calibration comparison technique was verified for the measurement of the characteristic impedance of the commercial CPW lines up to 110 GHz on the CS-5 alumina calibration substrate. The CS-5 substrate consisted of lumped standards (open, short, and load) as well as CPW line sets: a 150 µm long thru line, and four lines with lengths of 6550 µm, 1450 µm, 950 µm, and 500 µm. Its estimated effective dielectric constant is about 5.26. The substrate is 625 µm thick. In these experiments, the calibration substrate was placed directly on the metal chuck.

The verification strategy was built as follows: using the lumped load method, the capacitance per unit length C' the CPW line was extracted from:

$$C' \approx \Re\left(\frac{\gamma}{j\omega R_{LOAD}}\frac{1+\Gamma_{LOAD,Z_{LINE}}}{1-\Gamma_{LOAD,Z_{LINE}}}\right) \tag{5.1}$$

where $\Gamma_{LOAD,Z_{LINE}}$ is the load reflection coefficient corrected by the TRL calibration with $Z_{REF} = Z_{LINE}$; γ is the propagation constant of the line measured by the multiline TRL; R_{LOAD} is the resistance of the load. The component $G/\omega C$ from (2.25) was neglected.

To increase the extraction accuracy, R_{LOAD} was measured using an SMU with an accuracy better than 0.05 Ω. Therefore, the C' value was assumed to be the reference parameter. The characteristic impedance Z_{LINE} as well as other equivalent circuit

parameters of the line: conductance G', resistance R' and inductance L' per unit length were calculated from the known C' and the propagation constant γ using the LINEPAR program (see Chapter 2 and Fig. 2.3).

After that, the reference multiline TRL calibration was performed on RM8130, setting the calibration reference impedance to $Z_{REF} = 50\ \Omega$ and shifting the calibration reference plane to the probe tips.

Finally, the second-tier multiline TRL was performed on the examined alumina substrate. The characteristic impedance Z_{LINE} of the alumina CPW line was extracted from the second-tier error boxes and the line propagation constant γ (the product of the second-tier calibration) with the help of the ExtractZ0[5] program. Same here, the capacitance C', the conductance G', the resistance R' and the inductance L' per unit length was found from the measured Z_{LINE} (2.21) and (2.22).

To ensure the results, the same experiment was repeated for another CS-5 substrate that was measured on the second setup. Results are presented in Fig. 5.5.

The results led to four important findings:

1. The calibration comparison method is in a good agreement with the lumped load method up to 40 GHz;
2. Parameters extracted from the calibration comparison method fall apart above 40 GHz;
3. Below 40 GHz, capacitance C' and inductance L' per unit length are different for tested CS-5 substrates;
4. All four parameters extracted from the calibration comparison method show the same trend but have noticeable deviation between setups.

As discussed in [77], the variation of about 7% for the capacitance C' and about 5% for the inductance L' per unit length for two CS-5 substrates roots in the instability of the thin film fabrication process.

Calibration comparison results strongly deviate above 40 GHz for both setups because the cross section of the RM8130 CPW lines is not optimized for those frequencies. Therefore, I considered the frequency band from 40 GHz to 110 GHz to be out of the RM8130 specification for the calibration comparison.

The setup dependent “error patterns” that are noticeable for all parameters extracted from the calibration comparison can be attributed to the probe dependent calibration residual errors. Here, I compared two calibrations performed on very different CPW designs and material. Thus, the probe-design dependent parasitic effects such as crosstalk, coupling, radiation, propagation of the higher-order modes can be significantly emphasized. Residual errors are particularly well exhibited above the specification of RF8130.

[5] Both LINEPAR and EztractZ0 are available from NIST, Bolder CO, USA.

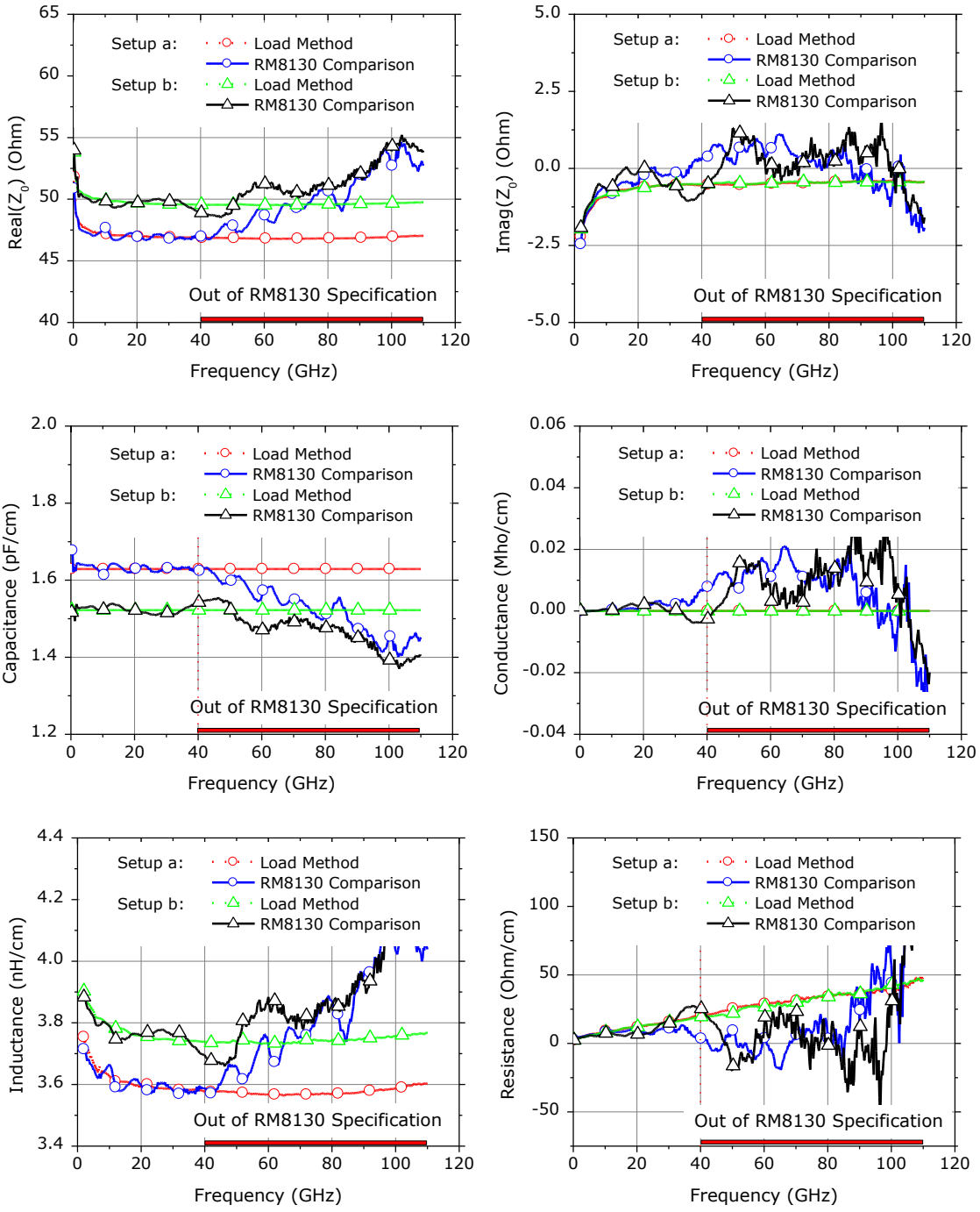


Fig. 5.5: Parameters of the CS-5 alumina CPW line extracted from the calibration comparison to the reference RM8130 calibration and the load method for two setups.

This experiment proved the following hypotheses:

1. The alumina CPW lines have negligible conductance loss;
2. The extraction of the coefficient $G/\omega C$ is not needed. Thus, the lumped load method is valid for accurate measurements of the capacitance per unit length C' of commercial alumina CPW lines;
3. The RM8130 cannot be used as a reference above 40 GHz.

Summarizing, it was proven that the reference calibration can be established using the commercial calibration substrates. This enabled accurate extraction of the line characteristic impedance Z_{LINE} on conductive substrates from the calibration comparison method. However, results indicate that there are some fabrication variations and probe-type design dependencies. This issue highlights the need for a reference material that is valid at least up to 110 GHz. That is why the characterized alumina substrates will be used as the reference for further experiments. For a particular alumina substrate, it is mandatory to measure the capacitance per unit length C' of its lines. Also, it is highly recommended to use RF probes of the same design for all experiments.

5.4 Results of Measurement of the Characteristic Impedance of the Line

5.4.1 IBM Advanced RF CMOS 8SF Process

In paper [77], the propagation constant and the characteristic impedance of custom line standards were obtained from the simulated and measured results. Both the lumped load and the calibration comparison method were used. For the calibration comparison, the reference multiline TRL calibration was established on both RM8130 (up to 40 GHz) and on the commercial alumina substrate CS-5 (up to 110 GHz). Before that, the characteristic impedance Z_{LINE} of the CS-5 CPW lines was accurately measured.

Also the capability of the 3D simulation was evaluated. The line was simulated with a simplified model using the 3D full-wave electromagnetic field simulation package Ansoft HFSS®. The 3D structure included all passivation and metal layers with interconnects simplified to solid bars. Simulation results yielded the electrical parameters of the transmission line including the propagation constant and the characteristic impedance. The experiments were carried out on data measured at IBM laboratory (Table 5.1, setup A).

Fig. 5.6 compares the simulated and the measured attenuation and phase constants. These parameters were measured directly through multiline TRL calibration, as shown in [22].

Fig. 5.7 shows the characteristic impedance Z_{LINE} of the same line obtained from four different experiments: EM simulation, lumped load method, calibration comparison method with the reference CS-5 calibration, and the calibration comparison method with the reference RM8130 calibration [56, 77]. All results are in a good agreement in the entire frequency range. The difference in the substrate material between the GaAs of the RM8130, the alumina, and the silicon appears to be successfully compensated by the calibration comparison method.

Next, the equivalent circuit parameters of the line were extracted to evaluate the impact of each method. It is important to note, that the lumped load method assumes that the capacitance per unit length C' is constant over frequency and that conductance losses

are negligible, i.e. $G/\omega C = 0$. Again, calibration comparison and the lumped load method are in a good agreement Fig. 5.8.

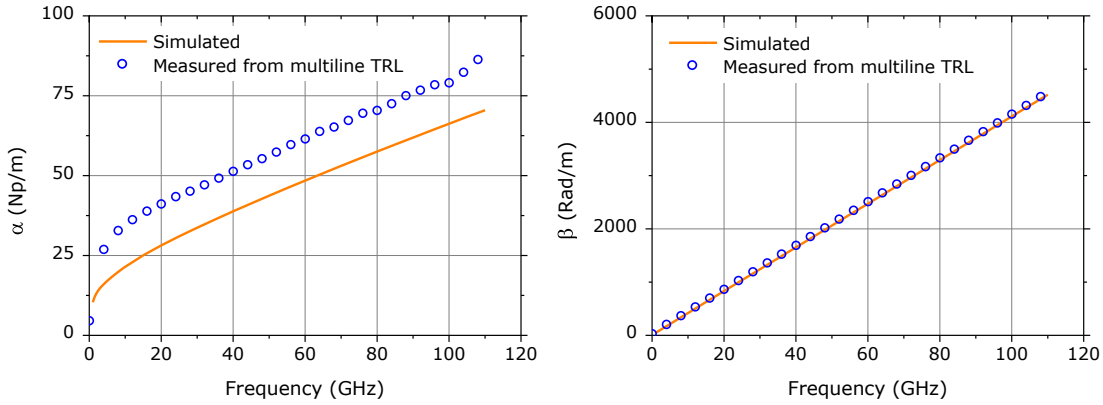


Fig. 5.6: Simulated and measured attenuation (left) and phase (right) constants of silicon line from the advanced IBM CMOS process.

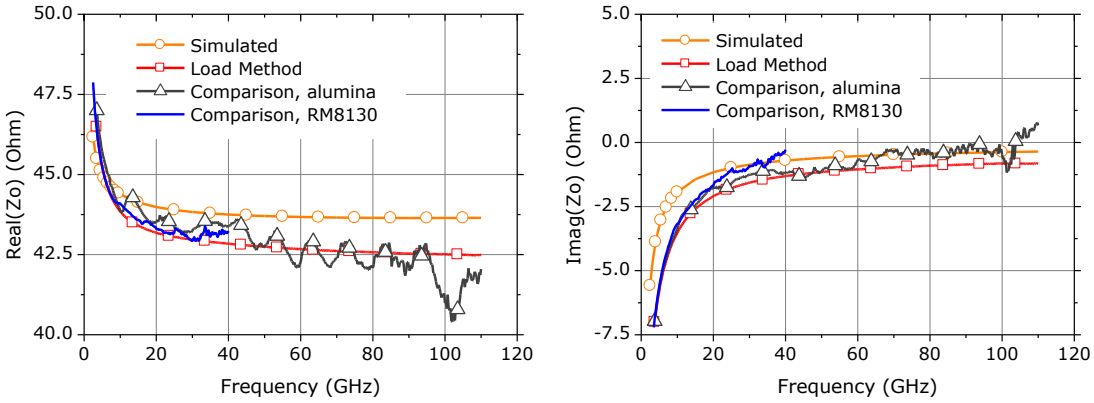


Fig. 5.7: Simulated and extracted real (left) and imaginary (right) parts of the examined silicon line characteristic impedance Z_0 from the advanced IBM CMOS process. Extracted data were obtained from the load method and the calibration comparison method to reference material RM8130 and alumina substrate. Comparison to RM8130 is limited in frequency to 40 GHz due to the specification of the used reference material.

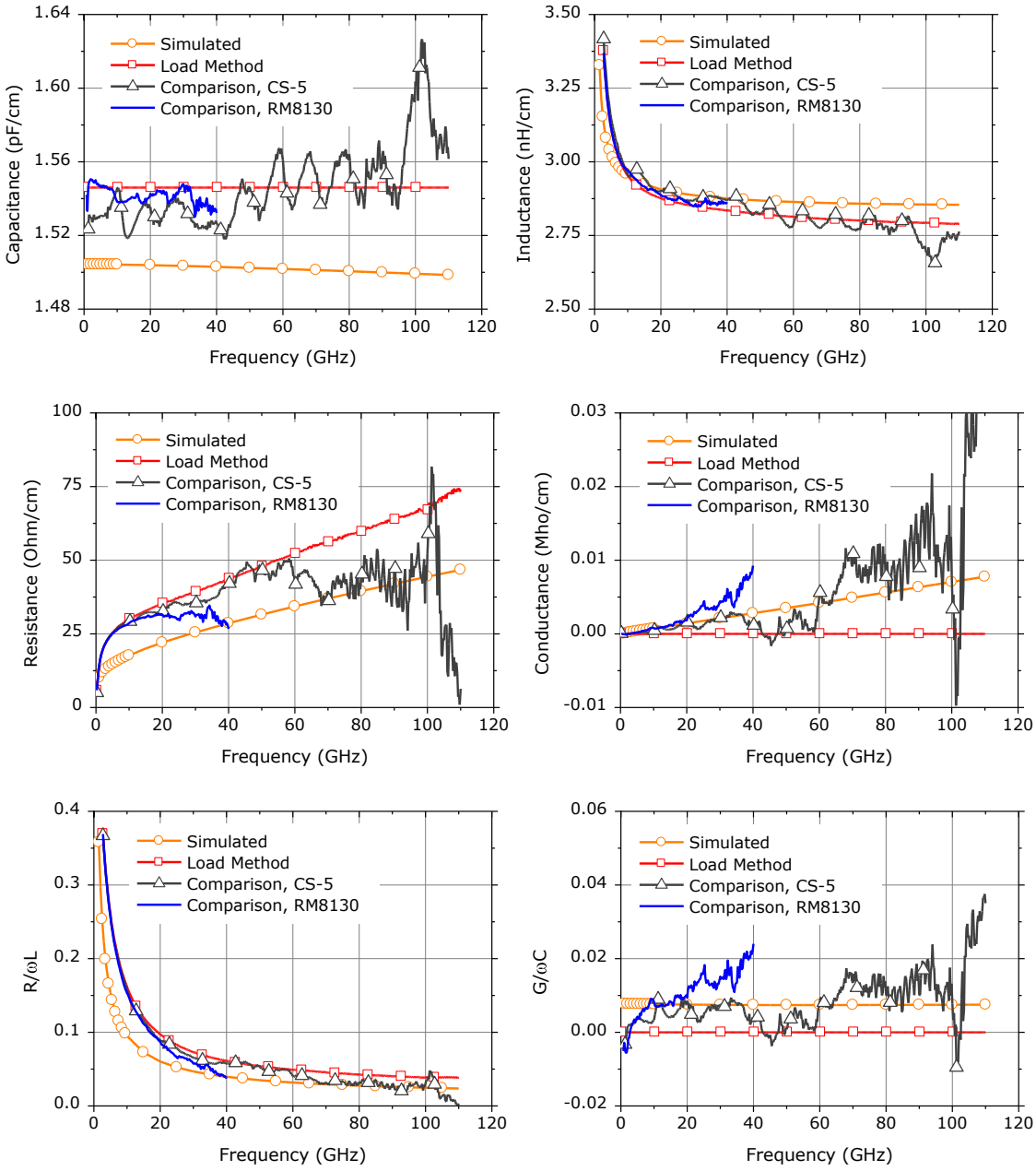


Fig. 5.8: Simulated and extracted cirquit parameters of the silicon line from the advanced CMOS IBM process. Extracted data were obtained from the load method and the calibration comparison method to reference material RM8130 and alumina substrate. Comparison to RM8130 is limited in frequency to 40 GHz due specification of the reference material used.

5.4.2 STMicroelectronics' BiCMOS9MMW Process

The similar measurements of propagation constant γ and the characteristic impedance Z_{LINE} were performed for the line implemented in the STMicroelectronics' BiCMOS9MMW test ship. Both the lumped load and the calibration comparison methods were used. Fig. 5.9 displays the propagation constant as well as the effective dielectric constant of the examined line. For comparison, the same characteristics of a commercial alumina substrate ISS 107-783A from Cascade Microtech are added to these graphs. The data for the ISS were obtained from a separate experiment.

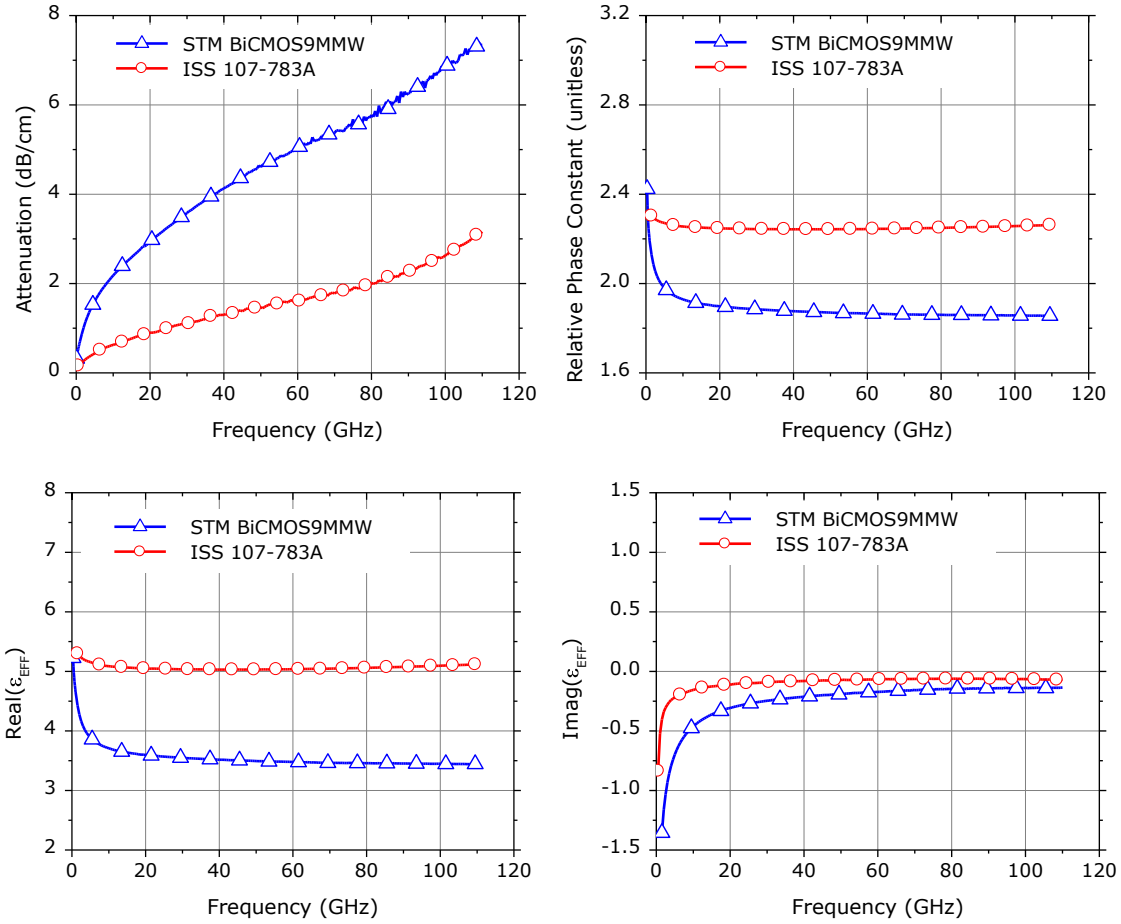


Fig. 5.9: The attenuation, the relative phase constant, and the real and the imaginary part of the effective dielectric constant of the calibration line standards measured by the multiline TRL. Comparison for the STMicroelectronic's BiCMOS9MMW process and the alumina calibration substrate ISS 107-783A from Cascade Microtech.

The real part of ϵ_{EFF} is 3.5 vs. 5.0 for the ISS line. The imaginary part is comparably small. The attenuation constant α is smooth and the relative phase constant β/β_0 does not change over the frequency. Therefore, one can conclude that BiCMOS9MMW lines support a quasi-TEM propagation mode at least up to 110 GHz. These measurement results are in a good agreement with published in [65].

Fig. 5.10 presents the characteristic impedance Z_{LINE} extracted from the calibration comparison (probe-tip multiline TRL on CS-5 as reference) and the lumped load method [57]. The measured capacitance per unit length is $C' = 1.262$ pF/cm.

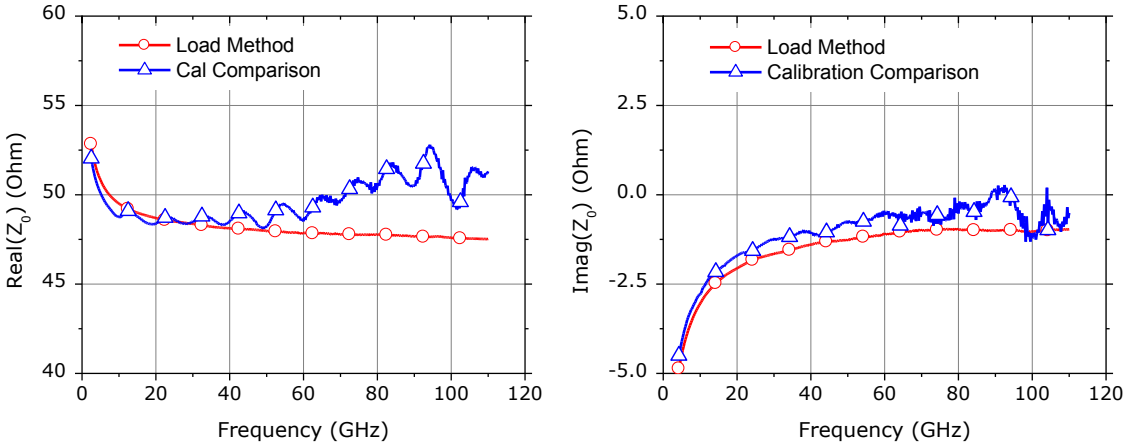


Fig. 5.10: Characteristic impedance Z_0 of line fabricated on ST Microelectronics' BiCMOS9MMW process. Results obtained from the lumped load and calibration comparison method on CS-5 alumina substrate.

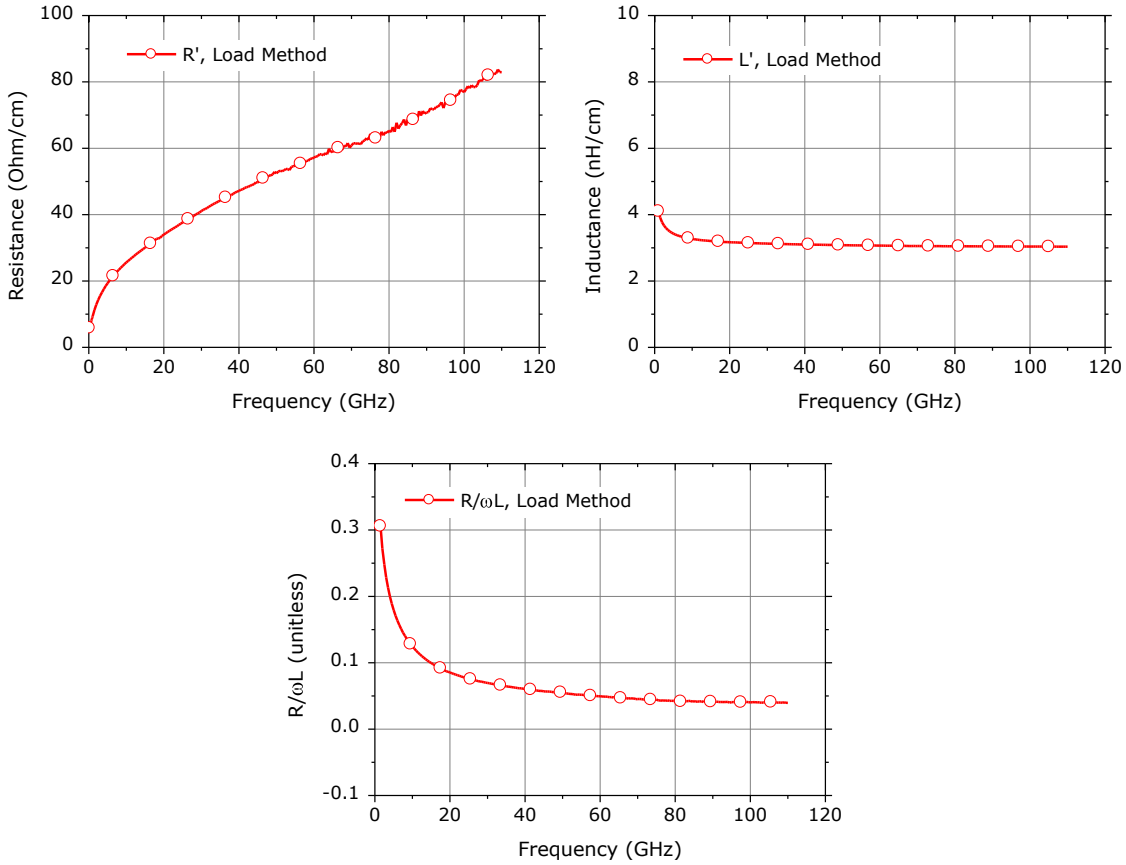


Fig. 5.11: Resistance R', inductance L' per unit length as well as R/ωL for the calibration lines from the ST Microelectronics' B5T BiCMOS process.

Finally, the line equivalent circuit parameters were extracted from the measured propagation constant and the characteristic impedance (based on the lumped load method): resistance R', inductance L' per unit length as well as $R/\omega L$ (Fig. 5.11).

A slight rippling was observed on the extracted parameters of the alumina CPW lines (Fig. 5.10). The same effect occurs on silicon lines in both IBM RF CMOS and STMicroelectronics' BiCMOS processes measured with respect to the first-tier reference calibration on alumina (Fig. 5.7, Fig. 5.10). In both experiments, the CS-5 calibration substrate and 110 GHz Picoprobes from GGB Industries were used. Possible reasons for such effects might be:

1. The high-resistivity absorbing layer that is placed under the ground conductors and extends them (design specific of the CS-5 CPW lines);
2. Non-ideal calibration boundary conditions, because the CS-5 was placed on the grounded metal chuck in this experiment;
3. The design of wafer probes.

Most importantly, however, the lumped load method demonstrates acceptable accuracy for determining the electrical characteristics of the transmission line standards on silicon up to 110 GHz. The success shown in this study is achieved by the design of the line standards on the silicon. The first metal level ground plane under the signal provides a dominant microstrip propagation mode in both technologies.

5.5 Definition of the Load Impedance

The EM simulation and the measurement methods were evaluated for characterization the load impedance Z_{LOAD} for various processes and layouts of the load standard [48, 56, 58]. As it was proven in [48], the load resistance is affected by fabrication process variability. Thus, it should be measured on every test chip.

The load reactance X_{LOAD} is defined for the reference plane located at the top metal. It is mainly represented by the equivalent reactance of the via stack (Fig. 4.8). Typically, the via stack reactance is relatively small and is of lumped nature.

If the reference plane is shifted to the probe tip end, the capacitance of the contact pads and the interconnect lines bring forth the largest contribution to the load reactance. This part is captured by the on-wafer calibration as a part of the systematic measurement errors and is calculated out.

5.5.1 Measurement Method

The on-wafer multiline TRL is the most accurate method to measure the load impedance and thus, its reactance. This approach provides broadband results. If the size of the test chip is limited, the number of the required lines can be reduced. The extraction of the

equivalent reactance of the load via stack should be done at frequencies of a well-conditioned TRL [56, 58].

The S_{11} and the S_{22} parameters of the load standard from the STMicroelectronics' BiCMOS9MMW process test chip are shown in Fig. 5.12. The data are corrected by the on-wafer multiline TRL. The calibration reference impedance was accurately set to $Z_{REF} = 50\ \Omega$. The measurement reference plane was located at the top metal level (M6 from this process) and was shifted 7 µm away from the center of the thru in both directions towards the pads (as discussed in Chapter 4, and shown in Fig. 4.8).

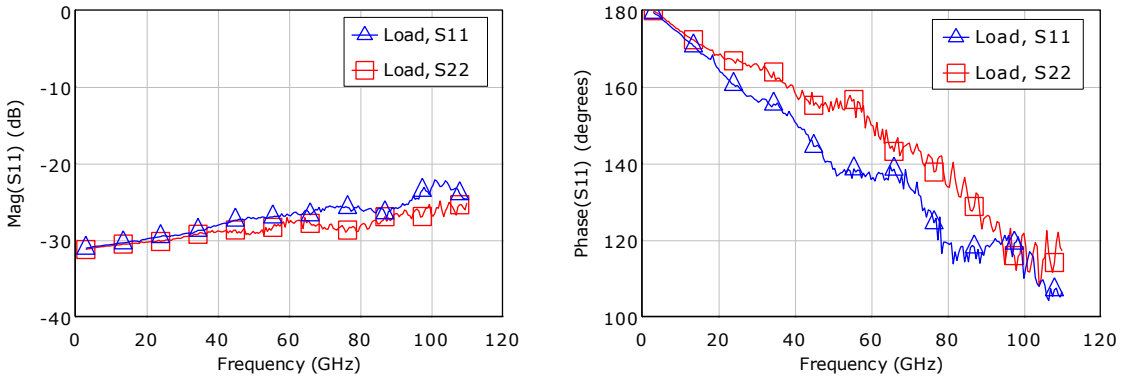


Fig. 5.12: The S_{11} and S_{22} parameters of the STMicroelectronics' BiCMOS9MMW process test chip load standard measured with the respect to the M6 multiline TRL.

As shown in [48], the load reactance is about 10 times less sensitive to the process instability than its resistance. That is why it can be assumed to be stable enough for a given process. It significantly simplifies measurement of the load impedance. For instance, the impedance of a particular load element can be recalculated "on-the-fly" from the known (nominal) reactance and the measured resistance R_{LOAD}.

It is not always required to extract the equivalent circuit parameters of a load model. In [48] we also proposed the following method: the real part of the load impedance can be normalized to the nominal value of its resistance R_{NOM}. For instance, the nominal resistance can correspond to a resistor laid out for $R_{LOAD} = 50\ \Omega$. Therefore:

$$R_{NORM}(f) = \frac{\Re(Z_{XX,NOM}(f) - Z_{YX,NOM}(f))}{Z_{XX,NOM}(f_0) - Z_{YX,NOM}(f_0))}, X, Y = 1...2; X \neq Y, \quad (5.2)$$

where Z_{NOM} are Z-parameters of the nominal two-port load and $Z_{NOM}(f_0) = R_{NOM}$.

The impedance $Z_{LOAD,ARB}$ of an arbitrary load element can be re-constructed from the measured resistance $R_{LOAD,ARB}$, as (Fig. 5.13):

$$Z_{LOAD,ARB}(f) = R_{LOAD,ARB} \cdot R_{NORM}(f) + j\Im(Z_{NOM}) \quad (5.3)$$

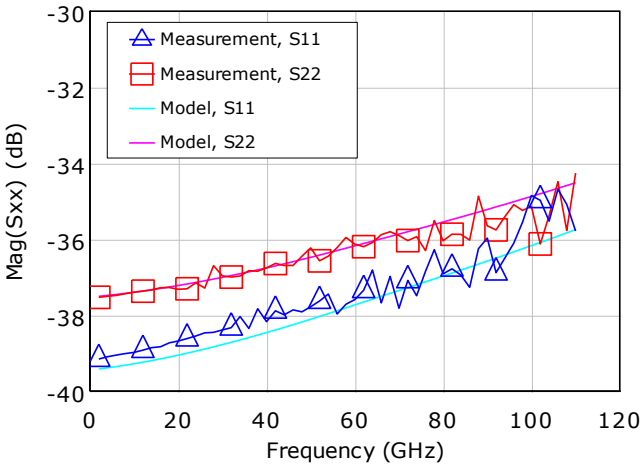


Fig. 5.13: Modeled and measured results of the load standard S_{11} and S_{22} parameters implemented in SiGe:C BiCMOS process from IHP Technologies.

5.5.2 EM Simulation of the Load Reactance

As it was demonstrated in [56], the simplified EM model of the load already provides an acceptable level of accuracy and is also a viable alternative for defining the load impedance. Indeed, the model does not require to include the whole element, instead only the via stack of the load resistor is needed. With other words, the simulation ports have to be located at the on-wafer calibration reference plane. It is much easier to simulate such a 3D structure accurately than the entire load element.

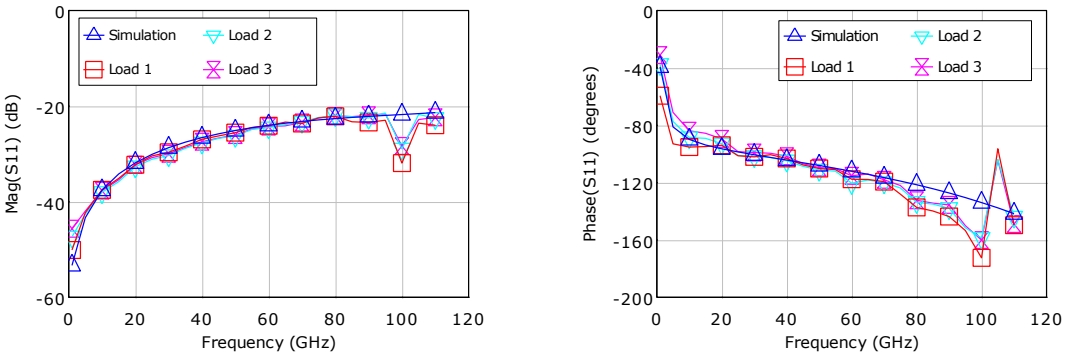


Fig. 5.14: The magnitude (left) and the phase (right) of the S_{11} parameter of three silicon load elements from the IBM advanced RF CMOS 8SF process. Comparison for the simulated vs. on-wafer multiline TRL calibration.

Fig. 5.14 compares simulated vs. measured results for the S_{11} parameter for the load from the IBM advanced RF CMOS 8SF process. The variation across the measured three

elements from the same chip is marginal and can be attributed to the contact repeatability error on aluminum pads. Also, as noted in [77], the measurement error at frequencies around 100 GHz is related to the specifics of the VNA used.

5.5.3 *Two Step De-Embedding for Measurement of Load Reactance*

The work [58] evaluated the possibility to use the probe tip calibration followed by the two-step open-short de-embedding for measurement of the load reactance. This method can be taken into consideration if it is not possible to implement the TRL standards on the test ship.

First of all, it proved that the tested load (from the BiCMOS9MMW test chip) can be assumed to be purely lumped at least up to 110 GHz. Thus, extraction of the equivalent load inductance can be successfully done at relatively low frequencies, i.e. below 40 GHz. At those frequencies, the two-step open-short de-embedding provides reliable results and makes the extraction procedure simple and practical. In our experiment, both the probe-tip calibration extended by the pad open, pad short (Fig. 2.11.a, Fig. 4.10) de-embedding and the on-wafer multiline TRL revealed good agreement for measured load reactance (Fig. 5.15). For this particular design of the load, the equivalent circuit mode is given by a series resistor R_{LOAD} and an inductor L_{LOAD}. It is valid up to 110 GHz. For the example shown in Fig. 5.15, the extracted parameters are $R_{LOAD} = 47.8\ \Omega$ and $L_{LOAD} = 7.8\ pH$.

A slight roll off of the measured real part of the load Z_{11} parameter might be caused by the extraction error. A simple one-port impedance element model was used for the load because the experiment was focused on the frequency range below 40 GHz (marked as “area of interest” in Fig. 5.15). This simple model does not account for crosstalk between measurement ports that increases with the frequency. But, for the frequency range of interest, all methods demonstrated a good agreement.

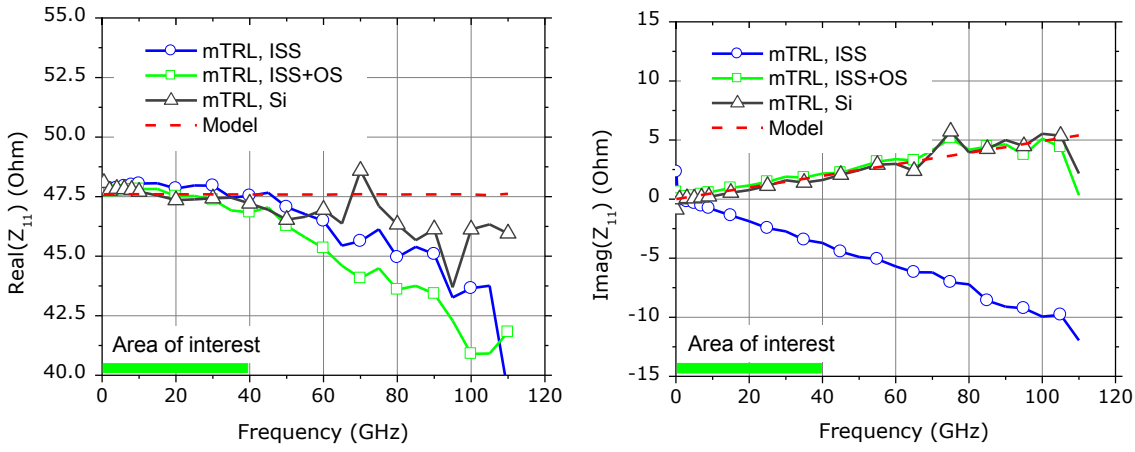


Fig. 5.15: The real (left) and imaginary (right) part of the Z_{11} parameter of the load from the STMicroelectronics’ BiCMOS9MMW process.

5.6 Conclusion

Several methods were developed suitable for measurement of characteristic impedance Z_{LINE} of the line and the impedance of the load Z_{LOAD} standards implemented on a silicon test chip. Both parameters are crucial for the successful and accurate on-wafer multiline TRL and the transfer TMR calibrations.

For the first time, the calibration comparison method was verified for the measurement of the characteristic impedance Z_{LINE} of the line for frequencies up to 110 GHz. Thus it became possible to establish a solid reference calibration on silicon.

Also, it was proved that a simple method based on the lumped load can be used for measurement of the line Z_{LINE} on silicon as well. If the calibration lines are designed properly (for instance, as on the IBM RF CMOS 8SF or STMicroelectronics' BiCMOS9MMW processes), the results of the lumped load method are valid over the entire frequency range (i.e. up to 110 GHz in my experiments).

Both methods were validated on the multiline TRL calibration kit implemented on the test chip from two different processes, RF CMOS and BiCMOS.

For the first time, the lumped load method was applied for measurement of the characteristic impedance of CPW lines from commercial calibration substrates and verified it against metrological reference material RM8130 up to 40 GHz. This work enabled the use of the calibration comparison method for measurement of the characteristic impedance Z_{LINE} of silicon lines above 40 GHz when conductive losses cannot be neglected.

The calibration residual errors caused by the RF probe design were identified. It was shown that they impact the results of the calibration comparison method. These effects call for future extensive and detailed investigation.

Several methods for measurement of the load impedance were developed and verified. It was proved that the load resistance can be measured "on the fly". Conventional SMUs that are connected to the RF probe by using the bias-T offer an acceptable accuracy for this kind of measurement. The load reactance depends on the load design and process specifics. It does not vary significantly with the process instability. Thus it can be either simulated or measured with respect to either the probe tip or the reference on-wafer TRL calibration. Each method was validated and it was found that they yield comparable results. The final choice depends on individual preferences for a particular process, the design of the load as well as on the size of the test chip.

The methods, experiments, and results demonstrated and discussed in this chapter formed a solid background for the implementation of the *in-situ* multiline TRL and the transfer TMR calibration methods for advanced RF silicon processes.

6 VERIFICATION METHODS FOR ON-WAFER CALIBRATION

Several methods can be applied to verify the accuracy of the *in-situ* calibration. It is always recommended to implement some transmission lines into a test chip to enable the reference multiline TRL. With the help of the calibration comparison method from [78], other *in-situ* calibration methods can be quantitatively verified against the multiline TRL reference. Often, especially in the phase of technology development, it is mandatory to achieve the highest possible calibration and thus measurement accuracy for devices. Also, technology development engineers should provide accurate PDK model parameters of the Back-End devices (including transmission lines, e.g. [65]). So, there are many benefits from implementing the multiline TRL structures into a test chip. However, in the mass production phase, the increase of the cost of test caused by additional space-intensive structures is not acceptable. Instead, cost-effective verification methods should be used for a qualitative verification of the accuracy of the *in-situ* calibration (e.g. [50, 52, 82]).

Both the multiline TRL and the transfer TMR were qualitatively verified and the results were published for IHP SiGe:C BiCMOS [48], IBM RF CMOS SF8 [56], and STMicroelectronics' BiCMOS9MMW [57-59] processes. For the first time, the quantitative verification of the transfer TMR was performed that was implemented on the IBM RF CMOS SF8 test chip up to 110 GHz. Results were reported in [56].

6.1 Verification of the multiline TRL

In Chapter 5, it was proved that the transmission lines from both IBM RF CMOS and STMicroelectronics' BiCMOS processes can be considered as supporting a single propagation mode up to 110 GHz. Also, two methods were demonstrated for accurate measurement of the line characteristic impedance Z_{LINE} for both processes. Therefore, the *in-situ* multiline TRL is justified to be the benchmark reference for quantitative accuracy verification of other methods. The reference impedance of the benchmark TRL is transferred to $Z_{REF} = 50\ \Omega$ after accurate measurements of the line characteristic impedance Z_{LINE}. Here, some qualitative verification results are presented for the multiline TRL that were not reported in the referenced publications.

The common qualitative verification technique of a self-calibration method (such as TRL) is the evaluation of the reflection coefficient of the reflect standard r_X from (3.33). The verification criteria are described using the example of the TMR method later. The results for the multiline TRL are presented in Fig. 6.1.

Also, the S-parameters of passive elements, such as calibration lines or de-embedding dummies, are good indicators of the calibration success.

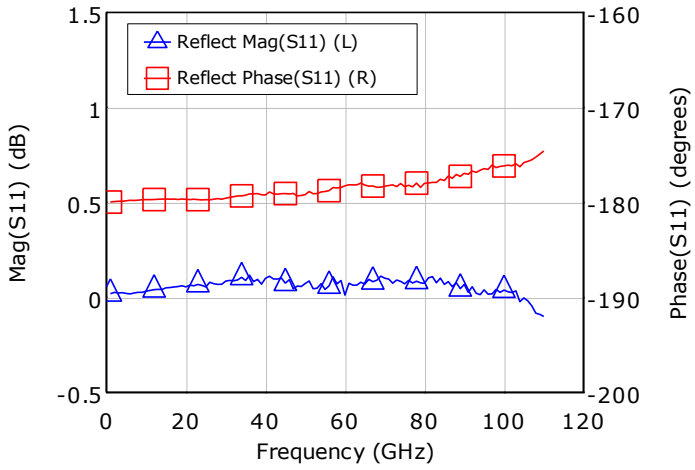


Fig. 6.1: The magnitude and the phase of S_{11} of the reflect (short) standard implemented on STMicroelectronics' BiCMOS9MMW test chip measured with respect to the on-wafer M6-level multiline TRL.

Fig. 6.2 exemplifies the return and the insertion loss of the thru standard implemented on the STMicroelectronics' BiCMOS9MMW test chip. The raw measurement results are corrected with probe-tip as well as with the on-wafer multiline TRL. The reference plane of the on-wafer calibration is located at the top metal level and is shifted 7 µm away from the center of the thru towards the probe tips. The comparison proves that the contact pad parasitic impedance and the parasitic contribution of the interconnect section are accurately captured by the systematic measurement error model of the entire system and are calibrated out. The calibration reference impedance of both probe tip and on-wafer multiline TRL is set to $Z_{REF} = 50\ \Omega$.

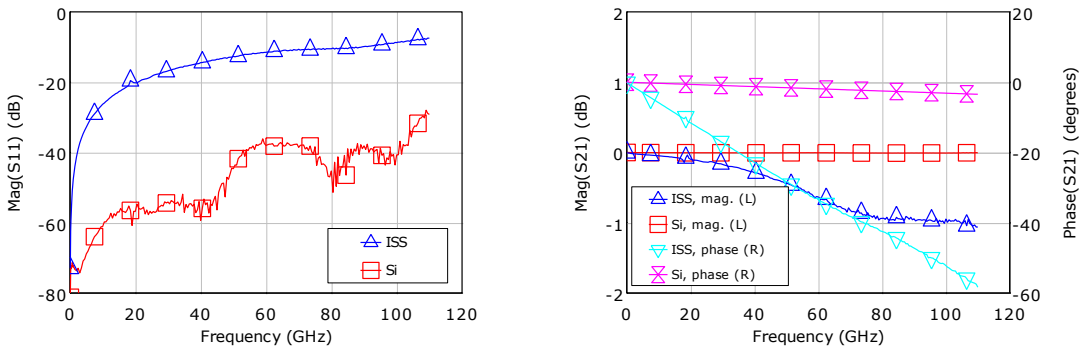


Fig. 6.2: The magnitude of S_{11} and the magnitude and phase of S_{21} of the thru standard standards implemented on STMicroelectronics' BiCMOS9MMW test chip measured with respect to the probe tip (ISS) and on-wafer M6-level (Si) multiline TRL.

The return and the insertion loss of all three lines from the test chip are given in Fig. 6.3. Here, the parameters are corrected by the on-wafer TRL under the same conditions.

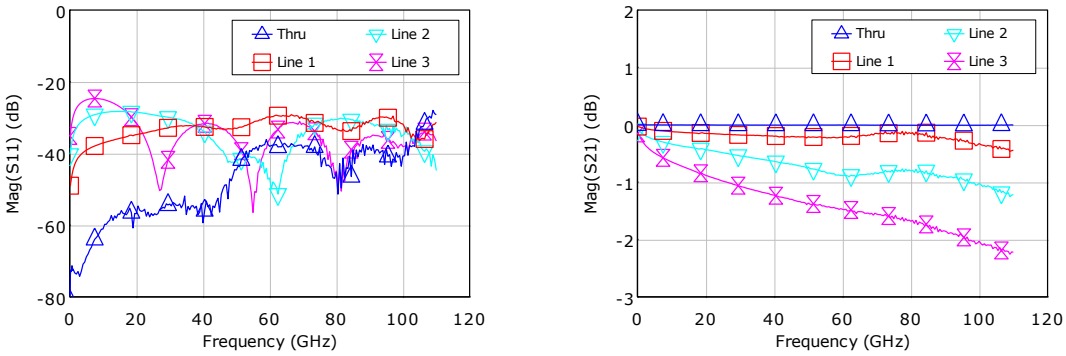


Fig. 6.3: The magnitude of S_{11} and S_{21} of the calibration line standards implemented on STMicroelectronics' BiCMOS9MMW test chip measured with respect to the on-wafer multiline TRL.

6.2 Quantitative Verification of the Transfer TMR

The quantitative accuracy verification of the transfer TMR was performed for the first time the on Si for IBM 0.13 µm RF CMOS SF8 process [56]. The experimental setup for the 110 GHz wafer-level measurements of the RF CMOS test chip included an Agilent 8510XF VNA, a semi-automated wafer-probe station Summit 12k, and 110 GHz wafer probes with a pitch of 100 µm from GGB Industries. The influence of contact repeatability on measurement data, calibration standards, verification elements, and evaluation transistor S-parameters was reduced by acquiring raw data (with error correction turned off) in three measurement runs. Measurement data from the VNA were recorded with proprietary data acquisition software developed by IBM and with commercial software SussCal. Off-line TMR and TRL calibration, error correction, and calibration comparison was performed using SussCal and MultiCal[6] software packages.

The following factors affect the results of the quantitative verification procedure:

1. Drift of the measurement system (basically, the drift of the VNA) within the experimental time;
2. Contact repeatability error on aluminum pads of the IBM RF CMOS SF8 process;
3. Accuracy of the reference calibration.

First, the system drift (instrument drift) was measured within the time interval of the DUT measurements using the calibration comparison technique and a commercially-available alumina calibration substrate. The probe contact repeatability error is

[6] Multical is available from NIST, Bolder CO, USA

significantly less than the measurement instrument instability within the experimental time (about eight hours) due to fabrication of the standards with gold contact pads. Therefore, it was assumed that the error defined from the calibration comparison method represented merely the instability of the measurement instrument.

Also, the contact repeatability error was quantified for probing on aluminum pads from three identical measurement series A, B, and C, of the same wafer-embedded calibration set. Obtained results showed that the error between the series A-B, B-C and A-C are comparable and that it is larger than the instrument drift. It follows that the contact repeatability on aluminum pads affects experimental results more than the test instrument instability.

Next, the characteristic impedance Z_{LINE} of the RF CMOS line standards was extracted from both the lumped load as well as the calibration comparison methods. The commercially available calibration substrate CS-5 and the NIST RM8130 were used as the reference for the calibration comparison method of measurement of Z_{LINE} for the reference multiline TRL on silicon (as shown in the previous chapter). Thus, the accuracy of the reference multiline TRL on silicon was ensured. The reference plane for the calibration comparison was set to the top metal level and the end of the thru standard. The reference impedance of the benchmark TRL was transferred to $Z_{REF} = 50\ \Omega$.

Finally, the on-wafer TMR was verified against the benchmark multiline TRL. Similar to the previous experiment on the RM8130 (Chapter 5), the difference between the examined transfer TMR and the benchmark multiline TRL is comparable to the system instrument drift and the contact repeatability error for measurements on silicon up to 110 GHz (Fig. 6.4), [56].

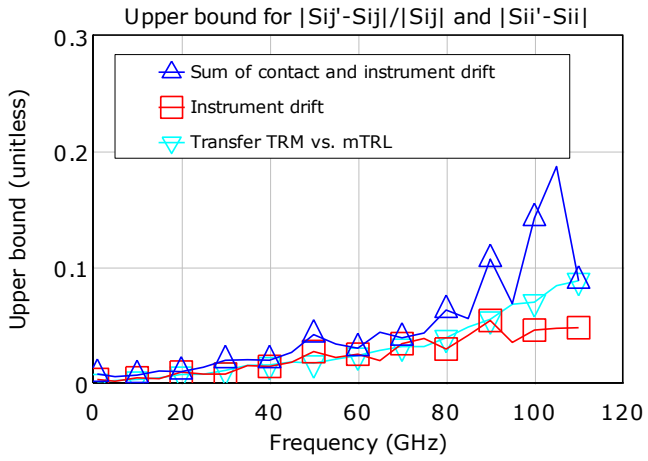


Fig. 6.4: The instrument drift, the sum of the instrument drift and the contact repeatability error as well as the accuracy verification of the transfer TMR calibration on the IBM RF CMOS SF8 test chip.

6.3 Qualitative Verification of the Transfer TMR

A qualitative verification of the *in-situ* TMR calibration can be applied when the reference calibration is not available.

6.3.1 Verification of the Reflect r_X

Similar to the TRL, the TMR routine does not require the reflect standard to be fully known. Thus, the reflection coefficient r_X of the reflect standard calculated by the self-calibration step is a good indicator if the algorithm failed by any reasons. There are three evaluation criteria for r_X:

1. Its phase should be homogeneous within the entire frequency range;
2. Its magnitude should not show any gain, i.e. it must not exceed 0 dB;
3. The magnitude of S_{XY} (for paired elements) represented should be less than one (or negative in dB scale) across the entire frequency range.

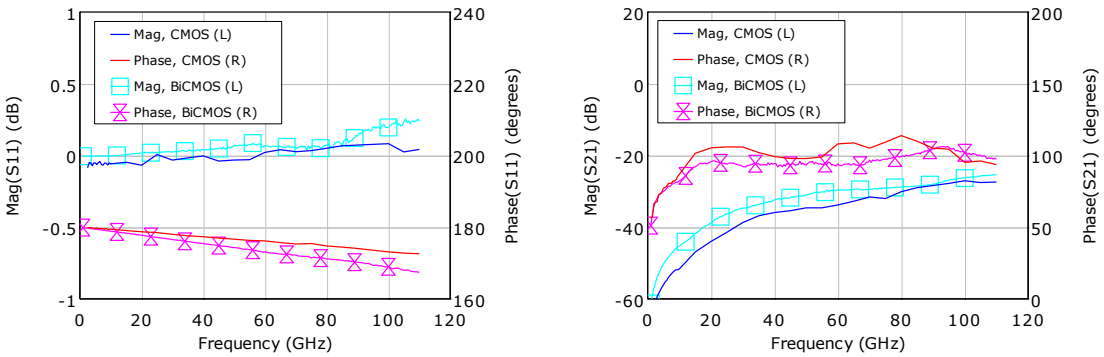


Fig. 6.5: The magnitude and the phase of S_{11} (left) and S_{21} (right) of the reflect standard from the IBM RF CMOS SF8 and the STMicroelectronics' BiCMOS9MMW test chips corrected by the transfer TMR calibration.

Fig. 6.5 compares the IBM RF CMOS SF8 and the STMicroelectronics' BiCMOS9MMW processes reflect standard S_{11} and S_{21} parameters corrected with respect to the *in-situ* transfer TMR calibration. Both measurements prove that the calibration is reliable within the entire frequency range. However, one observed a marginal increase of the magnitude of S_{11} by 0.15 dB from 85 GHz to 110 GHz in the BiCMOS experiment. This can be explained by the calibration residual error caused by the probe tip design[7] (Chapter 9). Anyway, this error is relatively small and is rather comparable to the typical contact repeatability error on silicon pads (Fig. 6.4).

[7] I used two different probe types for these experiments: Picoprobe from GGB for measurement of the IBM RF CMOS test chip and Infinity probes from Cascade Microtech for measurement of the BiCMOS9MMW test chip from STMicroelectronics.

6.3.2 *Verification for Open and Attenuator*

Accurate calibration aims at the exact definition of the reference impedance at both ports at $Z_{REF} = 50\ \Omega$. As it was showed in Chapter 2, the LRM-like procedures set the calibration reference impedance to the impedance of the load standard. If those loads are not equal at both VNA ports (e.g. due to the fabrication inaccuracy or the design specifics), the calibration reference impedance will be set inaccurately and will differ at the ports. Subsequently, the measurement of the same one-port device on different VNA ports gives results with either a positive or a negative offset from the expected value. The observed effect is often called "port asymmetry error". Fig. 6.6 gives an example of calibration residual errors of the conventional LRM calibration. It was performed with an asymmetrical load resistance of $R_1 = 49\ \Omega$ and $R_2 = 51\ \Omega$ and the symmetrical short as reflect. All standards were implemented on a commercial calibration substrate. The magnitude of S_{11} and S_{22} parameters on a verification symmetrical open element shows an offset of ±1.85 dB from the expected value of 0 dB.

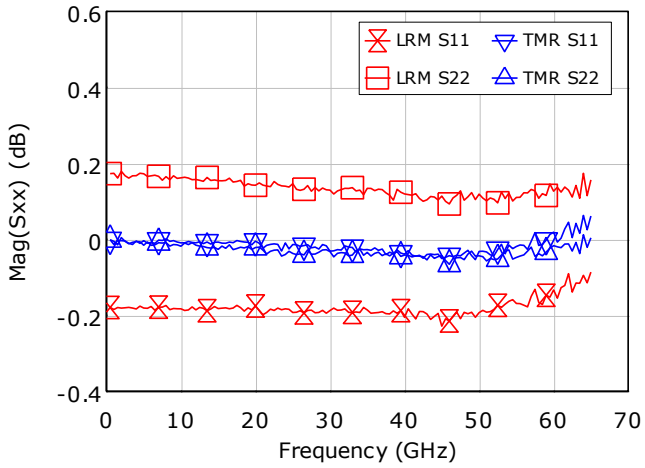


Fig. 6.6: The magnitude of S_{11} and S_{22} of a symmetrical open element. Data are corrected with respect to the conventional LRM and transfer TMR calibration performed with 1 Ω asymmety of the load resistance and short as reflect.

The method for the VNA ports symmetry verification was presented for the *in-situ* transfer TMR implemented on the SiGe:C BiCMOS process from IHP in [48]. Results from Fig. 6.7 proved that S_{11} and S_{22} of the symmetrical open and attenuator (Fig. 4.17 and Fig. 4.18) are in a good agreement. Hence, the transfer TMR algorithm has accurately compensated for the asymmetry of the load as discussed in Chapter 3 (see also Fig. 5.13, Attachment 13.1, Fig. 5 and Fig 6).

However, there is an "unsymmetrical zone" between 80 GHz and 105 GHz with the maximum error at 96 GHz of ±0.2 dB for attenuator and ±0.22 dB for open element. This is typically acceptable in practice for this frequency range. In [48], this effect was explained by the unsuspected simulation error of impedance of the load. This may also be caused by design errors of the load.

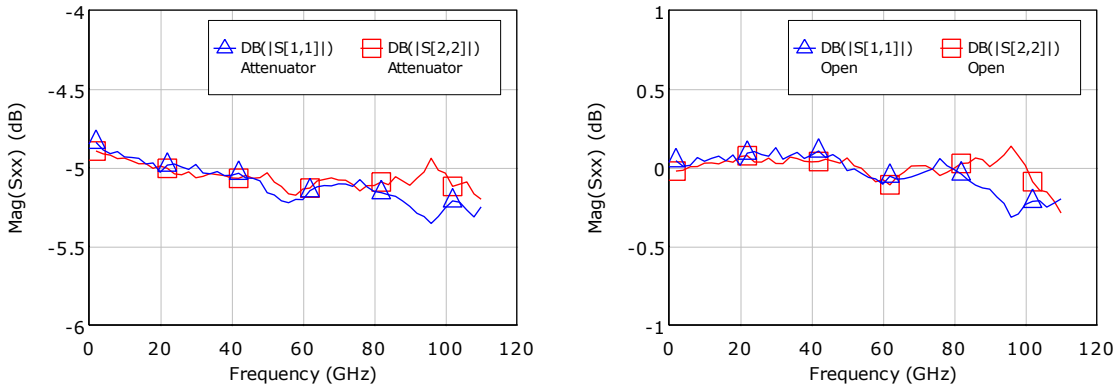


Fig. 6.7: Results of port symmetry verification for the transfer TMR (short as reflect) using the series attenuator and the symmetrical open from the SiGe:C BiCMOS IHP test chip.

6.4 Conclusion

For the first time, the transfer TMR calibration was qualitatively and quantitatively verified on challenging high performance RF silicon CMOS/BiCMOS technology up to 110 GHz. It was demonstrated that the difference of the benchmark multiline TRL and the TMR accuracy is comparable to the measurement system drift and the contact repeatability error.

It was shown that qualitative verification of calibration accuracy over the evaluation of the “port symmetry” is a good practical alternative to the calibration comparison method. Applying this method, the accuracy of the transfer TMR calibration can easily be verified in cases when the reference calibration is not available and/or when the use of the calibration comparison method is impractical or impossible. This may be the case during the in-line test or when implementing the calibration standards on the production test chip.

7 ADVANTAGES OF *IN-SITU* CALIBRATION

The benefits of the *in-situ* multiline TRL and the transfer TMR calibration methods were evaluated for every process: SeGe:C BiCMOS from IHP in [48], IBM RF CMOS SF8 in [56], and STMicroelectronics' BiCMOS9MMW in [57-59]. Several passive and active device parameters were used as test criteria. The advantages of the *in-situ* calibration over the conventional probe-tip calibration technique were demonstrated, which are:

1. Significant improvement of the measurement accuracy;
2. Simplification of the parasitic de-embedding.

This chapter gives an extensive comparison for devices of various geometries embedded in the STMicroelectronics' BiCMOS9MMW process modeling chip. Most of the results were not shown in the mentioned publications.

7.1 Choosing the Reference Probe-Tip Calibration Method for Comparison

Before verifying the *in-situ* calibration for characterization of active devices, it is necessary to have the benchmark probe tip calibration available for the entire frequency range. The commonly used SOLT method cannot be considered as a solid reference at frequencies above 20 GHz. I evaluated various probe-tip calibration methods and proved that only the multiline TRL is capable to establish well-defined calibration reference impedance and to place accurately the measurement reference plane to the desired location. Accuracy of other methods is limited due to imperfection of planar calibration standards and probe misplacement errors. Results were presented in [64] (Attachment 16.1).

It was a joint work with STMicroelectroncs (Crolles, France) and TUD (Dresden, Germany). I developed the methodology of the analysis, planned the work, wrote the major part of the paper and presented the results at a conference. I acquired the measurement data together with Paulius Sakalas (TUD) at the measurement system of the TUD CEDIC laboratory. I did parameter extraction together with Nicolas Derrier and Didier Celi from STMicroelectronics. The data analysis was shared between all co-authors.

Based on the conclusions of this work, the probe-tip multiline TRL was chosen as the benchmark against the *in-situ* calibration. For comparison, this chapter will use the data corrected by the probe-tip SOLT as it is the industry-standard probe tip calibration method [8].

7.2 Measurement Setup

The experiment on the BiCMOS9MMW chip was carried out on a broadband S-parameter measurement system from Cascade Microtech. It consisted of a semi-automated wafer-probe system Elite300™-AP, a pair of 110 GHz GSG Infinity Probes of 100 µm pitch and a fitting alumina calibration substrate (ISS), equipped with broadband 110 GHz PNA-X VNA and 4142B SMU from Agilent Technologies. The DUT input and output power levels (port 1 and port 2) were set to -35 dBm and -15 dBm to protect the DUT from overload. The output power was calibration on the port 1 to ensure the desired measurement conditions over the frequency range.

The measured data of the ISS and *in-situ* standards, the de-embedding structures and the test transistors were acquired in raw format (with the S-parameter calibration turned off). The calibration and error correction were performed by WinCal XE™[8], and proprietary IC-CAP[9] script outside of the VNA on a computer and for the same raw data set. This approach ensured a minimal impact of contact repeatability and instrument drift on the accuracy of experimental results. Device parameters were extracted using IC-CAP.

Seven characterization strategies were applied to the measurement data of four HBT geometries (Table 7.1 and Table 7.2).

Table 7.1: Calibration and de-Embedding Experiments

Experiment	Standards	Calibration Algorithm	De-Embedding
1	ISS	SOLT	two-step
2	ISS	LRRM	two-step
3	ISS	LRM+	two-step
4	ISS	mTRL	two-step
5	*in-situ*	LRM+	two-step
6	*in-situ*	mTRL	two-step
7	ISS	SOLT	six-step

The selected geometries represent a wide variety of DUT design, series and parallel parasitics. The comparison for DUT FoM's aimed at the following goals:

1. To show that *in-situ* calibration outperforms the conventional probe-tip calibration when the same two-step de-embedding is applied for shifting the measurement reference plane to the terminals of the intrinsic device (M6-level);

[8] WinCal XE is a product of Cascade Microtech, Inc.
[9] IC-CAP is a product of Agilent Technologies, Inc.

2. To compare the accuracy of two approaches: the most advanced six-step scalable de-embedding method augmented to the probe-tip calibration (Table 7.1, experiment 7) vs. the *in-situ* calibration augmented with the two-step de-embedding (Table 7.1, experiments 5 and 6).

The test included cold and biased measurement conditions of the DUTs.

Table 7.2: List of Measured Transistors

DUT	Geometry	Emitter width, µm	Emitter length, µm
DUT1	CBEBC	0.18	0.6
DUT2	CBEBC	0.18	5
DUT3	CBEBC	0.18	15
DUT4	C-5x(BEBC)	0.18	10
BUT5	CBE	0.18	5
BUT6	CBEB	0.18	5

7.3 Cold S-Parameter Results

The Base/Emitter C_{BE}, Base/Collector C_{BC} and Collector/Emitter (Collector/Substrate) C_{CE} capacitances were extracted from the cold-mode S-parameters of all DUTs. Fig. 7.1 compares the probe-tip SOLT and the reference multiline TRL calibration vs. the *in-situ* transfer TMR and the multiline TRL calibration methods (experiments 1, 4-6, Table 7.1) for three DUTs of the CBCBE configuration with Emitter width of W_E=0.18 µm and Emitter lengths L_E of 0.6 µm, 5 µm, and 15 µm (DUT1, DUT2 and DUT3, Table 7.2). The calibration data are de-embedded using the DUT-specific complete open and complete short elements. Similar, Fig. 7.2 gives the comparison results for the DUT5 and the DUT6 having the same W_E and L_E but different geometries (Table 7.2).

Only the *in-situ* calibration (i.e. both the transfer TMR and the multiline TRL) gives the expected RF signature of the π-equivalent circuit, which corresponds to the DUT in cold-S mode (0 V bias): the capacitances remain constant up to 110 GHz. The *in-situ* calibrations outperform probe-tip methods from 40 GHz for multi-finger and from 70 GHz for small transistors. Obviously, the two-step de-embedding impedance model does not capture distributed effects of parasitics between the probe-tip and the M1 reference planes (Fig. 4.2). The *in-situ* calibration includes these effects into the systematic measurement error model and thus calculates them out.

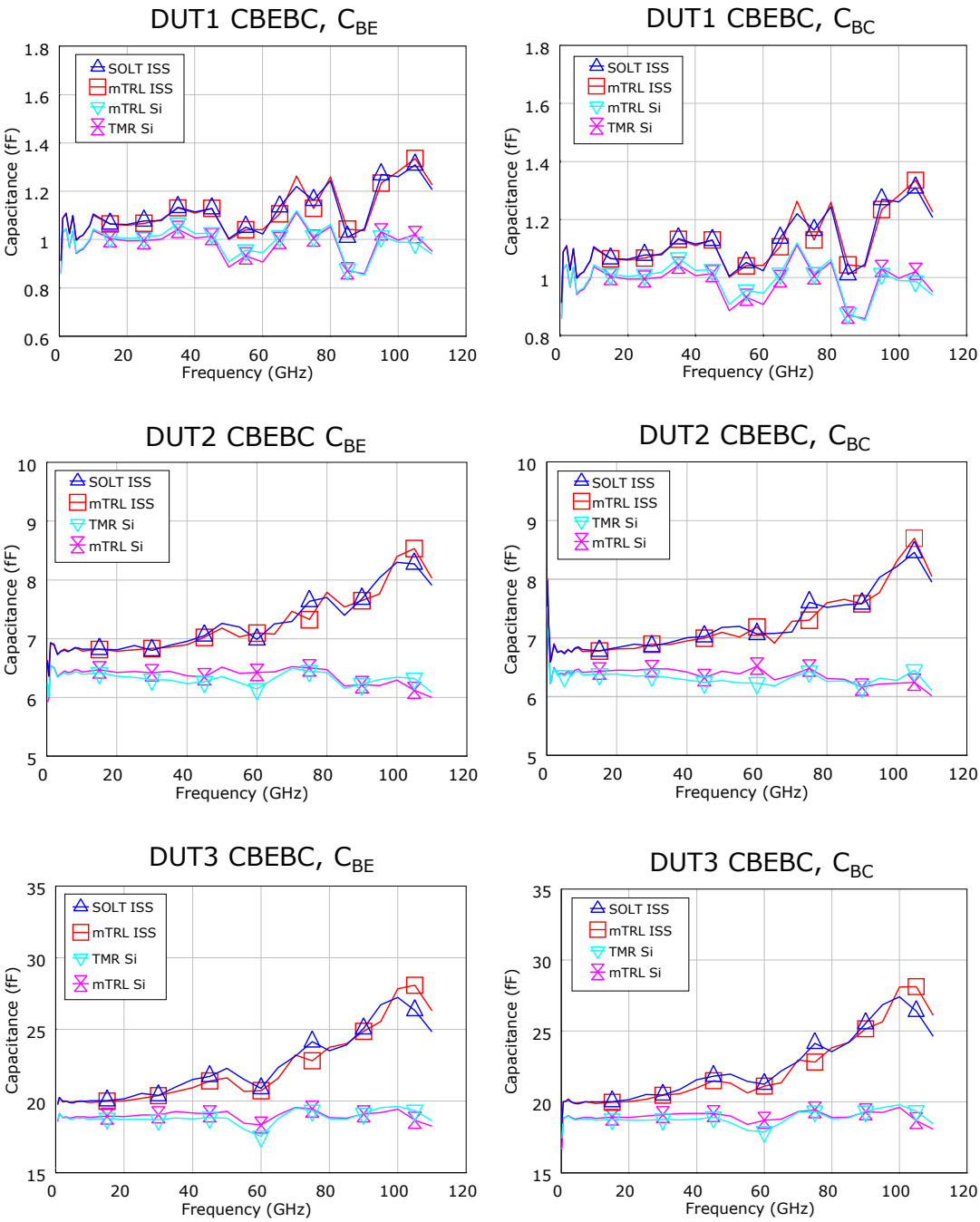


Fig. 7.1: Comparison of the probe tip SOLT and the multiline TRL vs. *in-situ* the transfer TMR and the multiline TRL for the Base/Emitter C_{BE} and the Base/Collector C_{BC} parameters measured for V_{BE}=V_{BC}=0 V for L_E=0.6 µm (top), L_E=5 µm (middle) and L_E=15 µm (bottom) CBEBC HBT with W_E=0.18 µm.

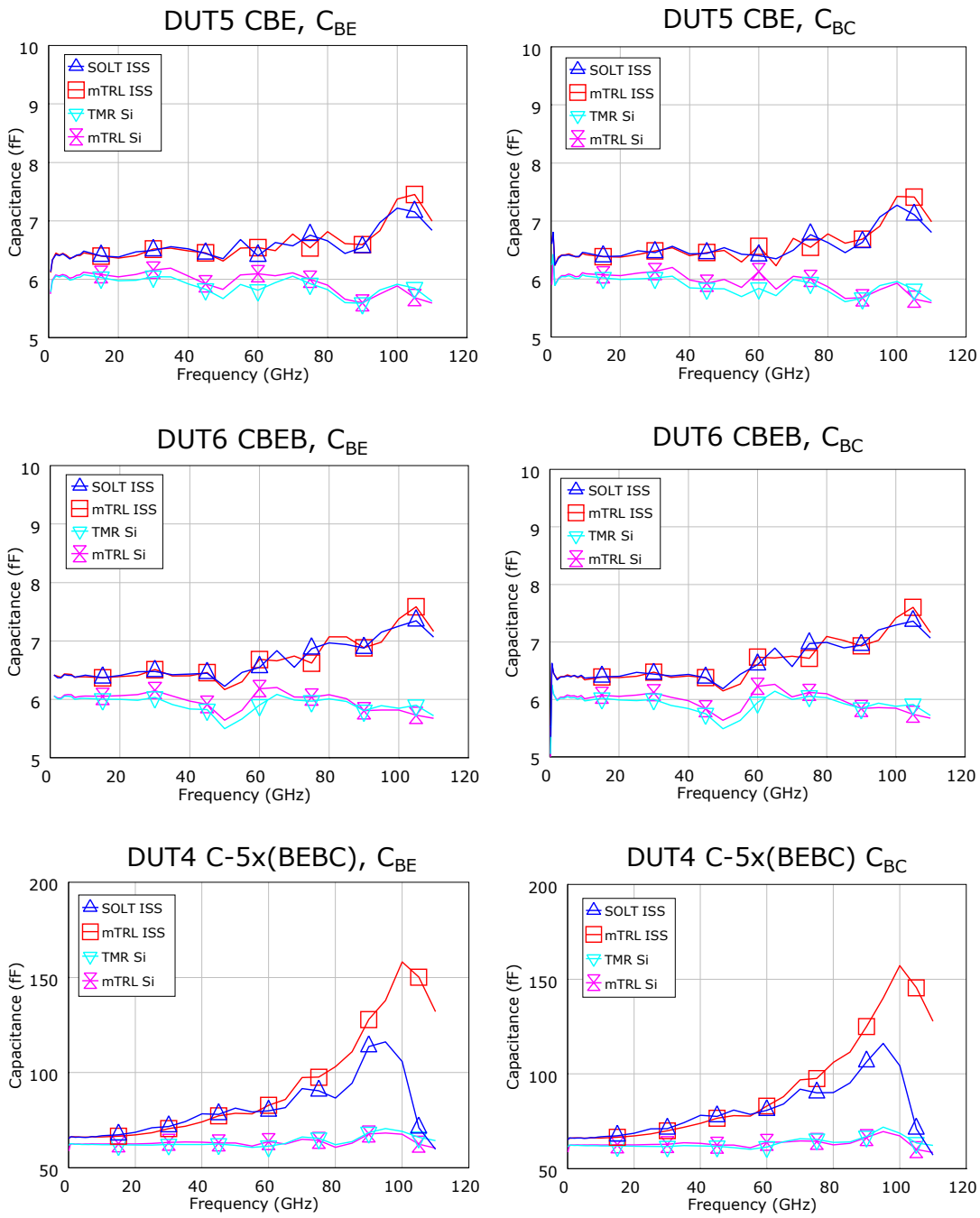


Fig. 7.2: Comparison for the probe tip SOLT and the multiline TRL vs. *in-situ* the transfer TMR and the multiline TRL for the Base/Emitter C_{BE} and the Base/Collector C_{BC} parameters of the CBE (top), the CBEB (middle) and HBT with W_E=0.18 µm and L_E=5 µm, and for the C-5x(BEBC) (bottom) HBT of W_E=0.18 µm and L_E=10 µm measured for V_{BE}=V_{BC}=0 V.

Also, the probe-tip calibrations show a slightly greater value of the extracted capacitances across all DUT geometries and experiments. This systematic effect requires further investigation for better understanding of its nature. Overall, this effect has negligible impact on the results.

Comparison for other probe-tip calibration methods revealed a similar relationship. Fig. 7.3 gives an example for the C-5x(BEBC) HBT (DUT4, Table 7.2) for experiments 1 to 6 (Table 7.1) [59].

In contrast to results presented in [64], the impact of the probe-tip calibration residual errors is not fully compensated by the two-step de-embedding in this experiment. It is explained as follows: the model of the VNA that was used for this experiment had a capability for accurate output power calibration at the mm-wave region (beyond 65 GHz) and for setting the power of the incident signal as low as minus 35 dBm. Thereby, the DUTs were not overloaded at mm-wave frequencies. It was possible to obtain more accurate results than in the experiment from [64].

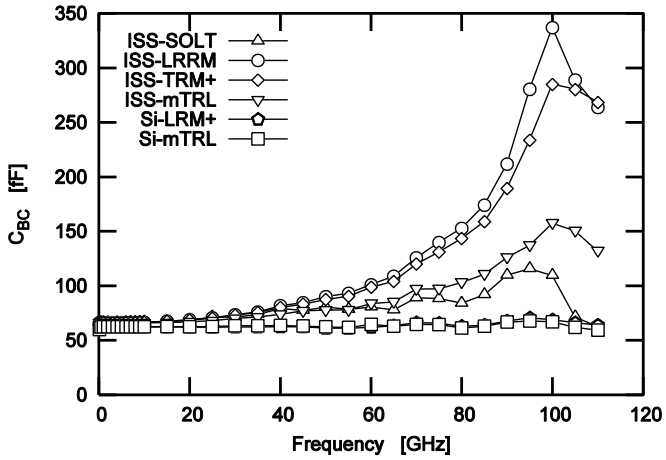


Fig. 7.3: Base/Collector capacitance CBC of the C-5x(BEBC) HBT of W_E=0.18 µm and L_E=10 µm measured at VBC=0 V.

7.4 Forward Mode S-Parameter Results

7.4.1 Y-Parameters

The DUT FoM Base/Emitter C_{BE}, Base/Collector C_{BC} and Collector/Emitter (Collector/Substrate) C_{CE} capacitances as well as maximum frequencies of the current gain f_T and the power gain f_{MAX} were extracted from the forward-mode S-parameters. Fig. 7.4 compares extracted C_{BE} of the CBEBC HBT with W_E=0.18 µm and L_E=5 µm (DUT2, Table 7.2) for the probe-tip multiline TRL, as well as the *in-situ* transfer TMR and the multiline TRL calibrations (experiments 4-6, Table 7.1) extracted from 20 GHz and 100 GHz data. As before, the *in-situ* calibration provided more reliable results (i.e. minimal parameter variation over the frequency) for the same two-step de-embedding from the complete open and the complete short dummies.

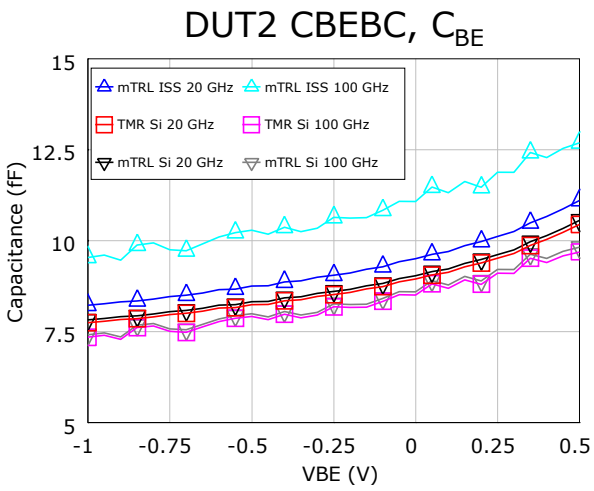


Fig. 7.4: Base/Emitter capacitance CBE of the CBEBC HBT of W_E=0.18 µm and L_E=5 µm measured for forward mode S-parameters extracted at 20 GHz and 100 GHz.

7.4.2 f_T and f_{MAX}

Fig. 7.5 shows peak f_T for a multi-finger device. Again, only the *in-situ* calibration methods give the expected results with constant f_T up to 110 GHz. While results for f_{MAX} demonstrated a comparable tendency, it is important to note that extraction of f_{MAX} is very challenging for advanced devices featuring small geometries. The port-to-port coupling that increases with the frequency affects the measurement accuracy of the DUT in the reverse mode. That is why crosstalk-corrected calibration methods (e.g. [83, 84]) may increase the accuracy of f_{MAX} extraction of small devices.

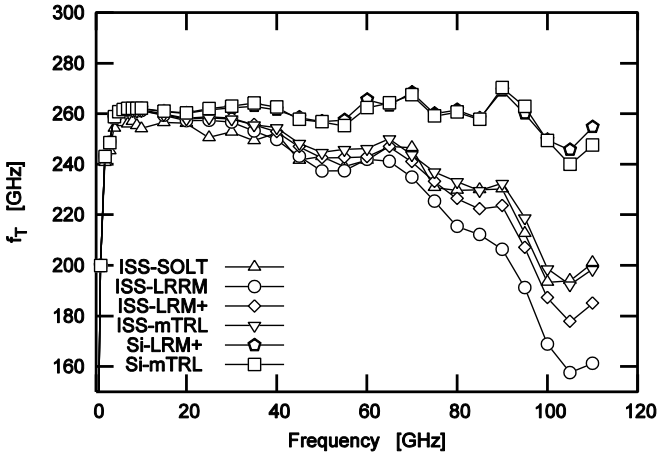


Fig. 7.5: Peak f_T (for JC=15 mA/µm2) vs. frequency [GHz] @VBC=0 V, for the C-5x(BEBC) HBT of L_E=10 µm.

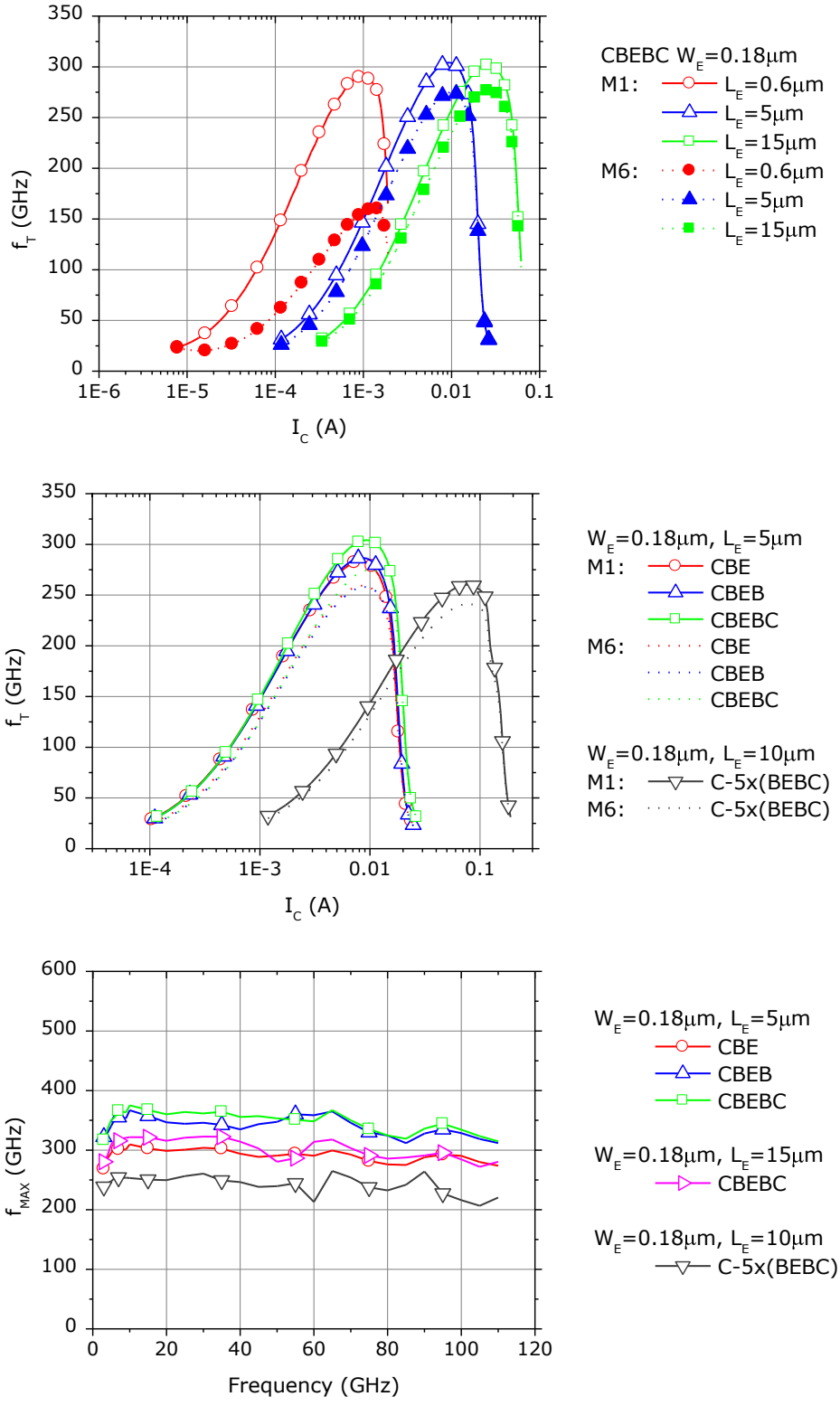


Fig. 7.6: f_T over i_C (top, middle) and f_{MAX} over frequency (bottom) for various device geometries extracted from the *in-situ* transfer TMR calibration extracted from f=20 GHz and V_{BE}=0.89 V respectively.

Fig. 7.6 compares f_T and f_{MAX} extracted from the *in-situ* transfer TMR calibration (experiment 5, Table 7.1) across various device geometries (DUT1 to DUT6, Table 7.2). f_T is presented for two locations of the reference plane: after the *in-situ* calibration(M6) and after the two-step de-embedding from the complete open and complete short dummies for each DUT (M1, Fig. 4.2). Here, the crucial point is that f_T is comparable for DUT1, DUT2 and DUT3 (Fig. 7.6, left). Often engineers may observe a decrease of f_T for short transistors and attribute it to so-called "3D effects" (e.g. [39]). Indeed, it is just a matter of how accurate and how close the measurement reference plane is shifted to the terminals of an intrinsic device. Results obtained here proved a very important statement from [59]: f_T of the intrinsic DUT is constant regardless of its length.

So far, results of different calibration methods followed by the same two-step de-embedding step were compared (experiments 1 to 6, Table 7.1). As it was discussed in Chapter 2, the six-step scalable de-embedding method can accurately capture parasitics from the probe tip to M1. Consequently, the next experiment explores in how far this method can improve the accuracy of the two-step de-embedding for the probe-tip calibration. Fig. 7.7 displays f_T of the same multi-finger transistor extracted from the experiments 1, 5 to 7 (Table 7.1). Indeed, the six-steps scalable de-embedding augmented to the less accurate probe-tip SOLT yielded results comparable to the *in-situ* calibration for the investigated frequency range. Y-parameters showed the same trend.

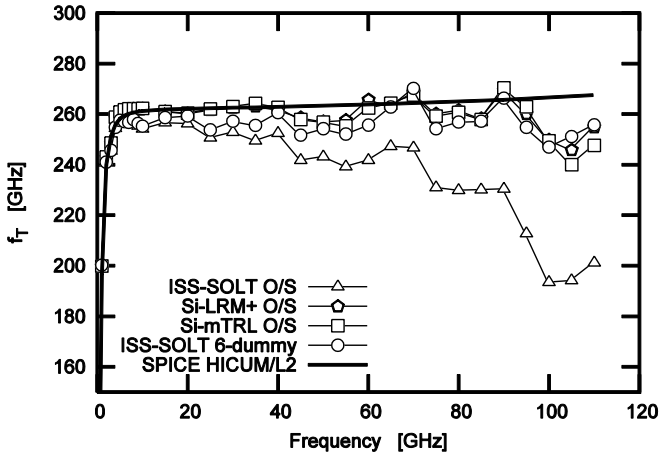


Fig. 7.7: Peak f_T (for J_C=15 mA/µm^2) vs. frequency @V_{BC}=0 V, for a five emitter finger HBT of L_E=10 µm, after the SOLT probe-tip calibration and complete open/complete short (white triangle) vs. six-step de-embedding (white circle), *in-situ* calibrations (white diamond and square), and the HICUM V2.30 compact model simulated with ADS software (solid line).

7.5 Comparison with a Compact Model

In [59], I also compared the extracted FoM with the HICUM Level2 compact model. I worked on this paper together with Nicolas Derrier from STMicroelectroncs (Crolles,

France) (Attachment 16.2). He extracted parameters of the compact model HICUM Level2 (L2) v2.30 [85, 86] for a test transistor DUT4 (Table 7.2) from DC and S-parameter measurements data, calibrated by the probe-tip SOLT and de-embedded using the two-step method. RF FoM f_T and f_{MAX} were computed at 20 GHz and used inside the extraction sequence, in order to avoid parasitic effects. ADS 2011.10 software was used to simulate the obtained model cards. The HICUM simulation results for f_T of the DUT4 are added to the Fig. 7.7. This comparison can be considered as an alternative proof, because the HICUM compact model is based on the device's physics. As we noted in [59], the Y-parameters demonstrated the same trend.

7.6 Conclusion

The numerous experiments on HBTs of various geometries revealed a substantial accuracy improvement of parameter extraction when using the *in-situ* calibration (multiline TRL or transfer TMR) followed by the simple two-step de-embedding. The *in-situ* standards are optimized to calibrate out the major part of the backend parasitics and to move the measurement reference plane to the M6 level in one step. It was proved that the remaining M6-M1 parasitics can be removed by a simple two-step de-embedding. A comparison with the compact model (HICUM V2.30) confirmed the findings.

The probe-tip calibration augmented by the six-step scalable de-embedding and the *in-situ* calibration augmented by the two-steps de-embedding yielded comparable results. Therefore, the choice of the method depends on the capability of the technology as well as on individual preferences.

The *in-situ* calibration requires some preparation work to characterize several electrical parameters of standards. In return, a simple two-step de-embedding can be applied. The probe-tip calibration demands an advanced six-step de-embedding with dummies easy to be realized. However, its application is cumbersome and needs additional silicon area.

8 ADDRESSING ISSUES OF ON-WAFER STANDARDS

8.1 How to handle standard properties that change over temperature

Device characterization for model development and IC design debug require measurement over a wide temperature range. For instance, a typical temperature test plan for silicon RF device characterization covers -40°C…+125°C with at least six temperature points. Advanced research requirements go far beyond these limits: down to 4°K and up to +500°C. That means that the *in-situ* calibration should be capable to deal with standards operating at those temperatures, e.g. standards with electrical characteristics that may change significantly with the temperature.

This is the opposite situation to a conventional probe-tip calibration. The auxiliary chucks that hold the calibration standards on a probe system are thermally isolated from the system thermal chuck (except special cryogenic probe systems). The calibration substrates are kept at relatively constant temperature conditions, ensuring that the electrical characteristics of planar standards remain almost the same during the temperature cycling (Fig. 8.1).

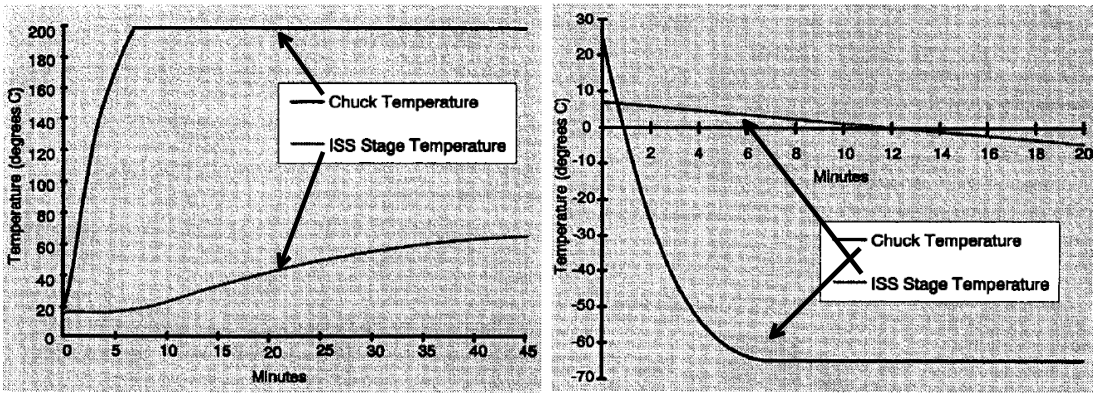


Fig. 8.1: Temperature relationship between the main system and the axially (ISS) chucks for a conventional RF probe system. The ISS stage is thermally isolated therefor the ISS standards stay at a relatively constant temperature conditions. Picture from [87].

Such a solution was developed in the early 1990s and since then it has remained the *de facto* industry standard [87]. There were no results or work previously published on the accuracy verification of the lumped-standard based calibration over temperature. That is why an initial investigation of this problem was done as well.

The thermal sensitivity of standards depends on the design and on the specifics of a particular semiconductor process. Therefore, it was decided to verify the accuracy of over-temperature calibration using the following strategy:

1. Investigate the temperature impact on characteristics of commercial CPW standards;
2. Analyze the probe tip calibration accuracy over multiple temperatures;
3. Identify the most and the least sensitive factors that influence the accuracy of different methods.

Here, the results of the probe tip calibration investigation previously published in [88-90] are presented. The outcome of this approach can easily be adapted to any custom calibration.

8.1.1 Experiment with Commercial Standards at Cryogenic Temperatures

The first paper on this topic addressed the negative temperature range, from room temperature down to 4 K [88] (Attachment 17.1). The experiments were carried out on a cryogenic wafer-level measurement system from SUSS MicroTech [91]. It was a collaborative work with FBH (Berlin, Germany) and TUD (Dresden, Germany). My contribution to this work was the idea, planning of the work, development of the test and verification methodology, data acquisition, some calculations and data analysis, as well as writing a paper. Ralf Doerner (FBH) greatly contributed to the calculation and data analysis of this work while Paulis Sakalas (TUD) assisted the measurement session.

The test setup allowed measurements up to 40 GHz. That was enough to get a good understanding of important aspects of the multiline TRL and the transfer TMR methods related with temperature variation. We measured the propagation constant γ, the capacitance per unit length C', and the characteristic impedance Z_{LINE} of the line as well as the resistance R_{LOAD} of the load standards over multiple temperature points. We used the CSR-8 calibration substrate from SUSS MicroTec in this experiment.

It was found that the attenuation constant α, the relative phase constant β/β_0 as well as the capacitance per unit length C' of the tested substrate decrease with the temperature. The characteristic impedance Z_{LINE} increases negligibly and is about 1% greater at 4 K than at room temperature.

As expected, we observed a decrease of the attenuation constant of about 50% at 4 K from its room temperature value. It is a common practice to neglect the loss of the thru standard for lumped-standard based calibration methods. This simplifies the calibration process but adds some errors. The decrease of the attenuation constant reduces this sort of errors.

A very stable and flat temperature coefficient of the CSR-8 load resistor was recognized. The resistance deviated from its room temperature value within +/-3%. This is a typical trimming accuracy for commercial load resistors across the substrate [69]. Thus, the load resistance of the test substrate remains within the limits of common specification.

Finally, the accuracy of the transfer TMR calibration was verified for the edges of the temperature region of +25°C and 4°K and under the conditions of conventional room temperature models and fully characterized thru and load standards at the temperature. Results obtained from the calibration comparison method (with the benchmark multiline TRL) proved that no additional efforts in characterizing standards are required for accurate transfer TRM calibration on CSR-8 substrate at cryogenic temperatures. It is expected that the same will hold for *in-situ* standards, except the load resistance R_{LOAD}. It may be more sensitive to temperature and might require a correction.

8.1.2 Experiment with Commercial Standards at High Temperatures

The investigation was continued for a high temperature range. The results were presented at the 71st ARFTG Conference where the paper received the Best Interactive Forum Paper Award [89] (Attachment 17.2). For this work, I developed the idea, test and verification methodology, planned the work, and performed some calculations and data analysis, and was responsible for writing the paper. Ralf Doerner (FBH) did the experimental measurements and provided the calculation and data analysis.

The results for cryogenic temperatures reported in [88] where measured with the cryogenic model of the |Z|-Probe from SUSS MicroTec. Because we did not have an alternative RF probes for measurement at cryogenic temperatures, the question whether the probe design had any impact on the extracted characteristics of standards remained unanswered.

So, first of all, two identical experiments were made. The attenuation constant α and the relative phase constant β/β_0 were measured at room temperature and at 150°C for the CSR-8 substrate, while using two different probes of the same configuration: |Z|-Probe from SUSS MicroTec and Picoprobe from GGB Industries (referred to as “probe P” in the article). It was demonstrated that the impact of the probe design is negligible for these experiments.

An ISS 101-190 substrate from Cascade Microtech was included to the experimental series (referred to as “substrate I” in the article). The setup had a measurement capability of 50 GHz and allowed testing from room temperature up to 150°C.

This work proved the previous statement that the characteristic impedance Z_{LINE} of the alumina CPW line decreases with increasing temperature. The temperature dependence of the attenuation constant α and the relative phase constant β/β_0 is in the same order of magnitude for both tested substrates. However we identified much higher temperature instability of the load resistance R_{LOAD} for the ISS 101-190. For the tested ISS, the extracted RTC was 92.9 ppm/°C while the CSR-8 demonstrated RTC=16.0 ppm/°C. This value is quite similar to the RTC=10.2 ppm/°C extracted from the measurement data of another CSR-8 substrate, presented in [88]. Such relatively high

variation of the load RTC is caused by differences in the design of standards and manufacturing technologies used by both vendors. If it is not taken into consideration, it affects the accuracy of the lumped-standard based calibration.

8.1.3 Sensitivity Analysis of Over-Temperature Probe-Tip Calibration for Multiline TRL, Transfer TMR and LRRM Methods

Changes in the electrical characteristics of standards over temperature may impact accuracy of various calibration procedures in different ways. For instance, the propagation constant γ of the line is automatically measured within the TRL algorithm. Therefore, TRL should be irrelevant to the variation in γ. Yet, it is sensitive to the line characteristic impedance Z_{LINE} as it leads to variation of the calibration reference impedance Z_{REF}.

The reference impedance of the lumped-standard based methods (such as transfer TMR and LRRM) is defined by the impedance of the load standard Z_{LOAD}. Moreover, the characteristic impedance Z_{LINE} of the thru and its propagation constant γ also contribute to the calculation of the reference impedance Z_{REF} of both TMR and LRRM methods, as it was showed in Chapter 2 (see also Fig. 3.2). Therefore, the accuracy of the over-temperature TMR and LRRM methods is affected by variations of three parameters: the impedance of the load Z_{LOAD}, the characteristic impedance Z_{LINE} and the propagation constant γ of the thru. The quantitative analysis of the contribution of certain standards to the overall accuracy of over-temperature S-parameter calibration methods has not yet been investigated. That is why I developed a practical method and concluded with recommendations on how to address the variation of electrical properties of standards across wide temperature ranges in the paper [90] (Attachment 17.3). I defined the scope of the work, developed the concept of the investigation, did several calculations, performed the data analysis, and wrote the major part of the paper. Ralf Doerner (FBH, Berlin) acquired all measurement results, did the major part of calculation as well as data analysis. Gavin Fisher (Cascade Microtech) contributed to some calculation results as well as to the preparing of the final manuscript.

The multiline TRL, the transfer TMR and the LRRM methods were investigated up to 50 GHz and for the temperature range from +25°C to 150°C. The frequency and the temperature range were limited by the capability of the FBH measurement setup.

For the considered experimental setup, it was found that the lumped-standard based calibration methods were less sensitive to temperature. In addition, it was shown that the load resistance R_{LOAD} is the main influencing factor for both LRRM and the transfer TMR methods. Therefore, a simple correction for resistance $R_{LOAD}(T)$ for a given temperature T can improve the calibration to the required level of accuracy:

$$R_{LOAD}(T) = R_{LOAD}(25) + \frac{RCT\ R_{LOAD}(25)(T-25)}{10^6}, \qquad (8.1)$$

where RTC is the Resistor Thermal Coefficient of the load resistor, ppm/°C; $R_{LOAD}(25)$ is the initial resistance value measured at room temperature, $T = 25°C$. In this case, $R_{LOAD}(25) = 50\ \Omega$.

Addressing temperature variation of the R_{LOAD} reduced overall TMR calibration error from 2.2% down to negligible 0.6%. Correction for α and Z_{LINE} of the thru only had a marginal effect.

All wafer-level systems configured for the electro-thermal characterization of semiconductor devices include several SMUs. They are used for biasing the DUT to measure its output I/V characteristics as well as the hot (biased) S-parameters (Fig. 2.6). As it was show in paper [89], the resistance R_{LOAD} of the load standard can be measured at the current temperature over the RF probes and the measurement system's bias-Ts "on-the-fly". Such configuration yields sufficient measurement accuracy. Thus, there is no need for the definition of the load resistor RTC prior to calibration.

The detailed description of the "on-the-fly" correction of electrical characteristics of a standard at a given temperature is also given in the patent application DE102009029906 [92]. This method can successfully be applied for other types of calibration substrates, temperature and frequency ranges, as well as to the *in-situ* (on-wafer) calibration elements.

8.2 Impact of the Fabrication Inaccuracy of Custom Standards to the Accuracy of DUT Parameter Extraction

Instability of the fabrication process leads to variation of electrical parameters of custom calibration standards and reduces accuracy of calibrated measurement results. Here, one deals with the situation similar to the already discussed one in the previous section (the over-temperature calibration). The characteristic impedance Z_{LINE} of the line and the load resistance R_{LOAD} vary between different shots (test chips) on one wafer, but also from wafer to wafer.

To evaluate this effect, the load resistance R_{LOAD} was measured and the capacitance per unit length C' of the line standards was extracted on a test wafer of the STMicroelectronics' BiCMOS9MMW process. Five test chips on different locations were selected to have the widest possible parameter distribution across the wafer (Fig. 8.2). The measured and extracted results are presented on the Fig. 8.3.

Based on this test, the conclusion was made that the variations of C' and R_{LOAD} were not correlated to each other. That means that capacitance per unit length C' should be measured on every test chip for an accurate definition of the TRL reference impeadance Z_{REF}.

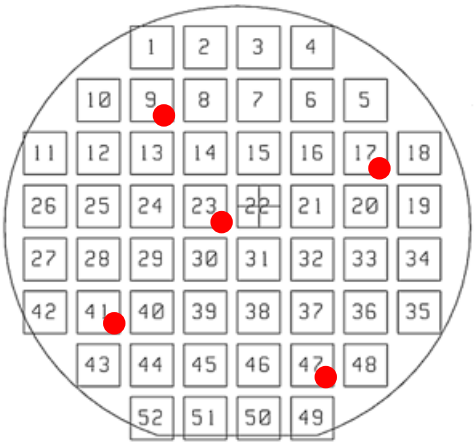


Fig. 8.2: Test shots of the STMicroelectroncs' BiCMOS9MMW process

All known measurement methods for the characteristic impedance Z_{LINE} of the line are time consuming. They require multipe calculations which are difficult to automate. The intermediate results require evaluation and validation by the operator. Moreover, the capacitance per unit length C' measured at NIST and supplied with every reference material RM8130 is defined with an accuracy of up to the fifth digit after comma. It is very challenging to achieve the same level of accuracy at normal laboratory conditions and on the typical wafer-level RF device characterization system, especially for silicon processes. The contact repeatibility on the aluninum pads is significantly worse than on gold, as I showed in Fig. 6.4. Therefore, it is cumbersome to implement the on-wafer multiline TRL into the in-line device characterization workflow.

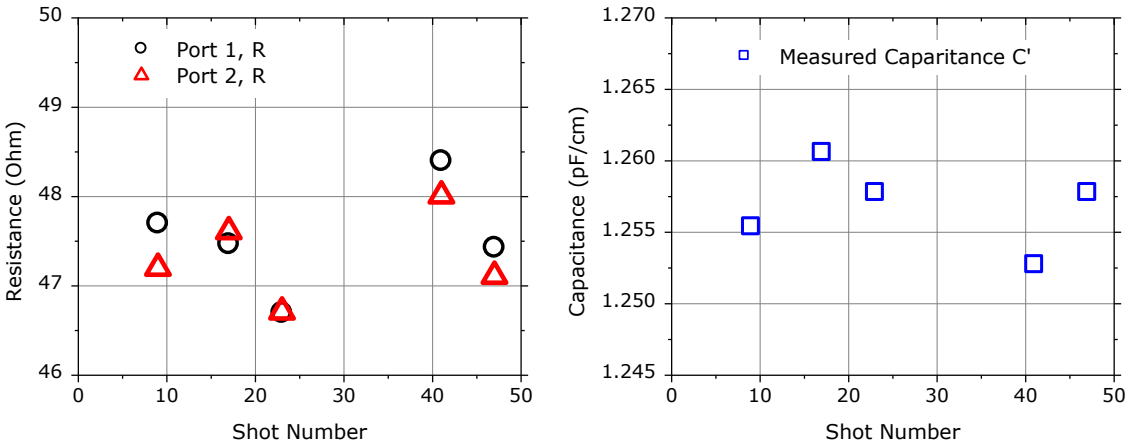


Fig. 8.3: Variation of the load resistance (left) and the extracted capacitance per unit length (right) of the load and line standards over five shots for one wafer of the STMicroelectronics' BiCMOS9MMW process.

Further, potential errors of transistor parameter extraction were investigated for the multiline TRL calibration when the calibration reference impedance Z_{REF} was not accurately measured. The analysis method and the results are given in [93] (Attachment 17.4). This work evaluated multiline TRL implemented in two processes: GaAs from FBH and BiCMOS9MMW from STMicroelectronics. I developed the analysis methodology, planned the work, acquired data for the BiCMOS process, did a part of calculations and parameter extraction, performed the data analysis with my co-author Ralf Doerner (FBH, Berlin) and wrote the major part of the conference paper. Ralf Doerner acquired the data for GaAs process and did the major part of calculations.

We investigated the accuracy requirements of the measurement of the characteristic impedance Z_{LINE} of the line using the lumped load method from [73] on GaAs and silicon processes for parameter extraction of passive and active devices. It was demonstrated that load resistance R_{LOAD} required for the extraction of the line capacitance per unit length C' can be measured with an accuracy of up to the second digit after comma. This corresponds to the measurement capability of a conventional wafer-level RF device characterization setup equipped with the SMUs and bias-Ts.

Also, it was shown that the transformation of the calibration reference impedance to $Z_{REF} = 50\ \Omega$ was not needed for extracting equivalent junction capacitances of a tested device for a given level of uncertainty of 10% and for the tested processes. Both findings proved that the implementation of the *in-situ* TRL into a characterization workflow in the investigated processes is significantly easier than we originally expected.

8.3 Conclusion

In this chapter, the analysis of the specific problems of the *in-situ* RF calibration was made. It included the instability of the electrical characteristics of standards due to temperature changes and inaccuracy of the fabrication process. These problems do not arise for the conventional probe-tip calibration. That is why they had never been investigated before.

It was demonstrated that it is necessary to know the actual resistance of the load R_{LOAD} on every calibration chip and at every calibration temperature, because the load resistance has the main impact on accuracy of the transfer TMR calibration. Also, it was shown that the unknown R_{LOAD} can be measured over the bias-Ts using the RF probes and the SMU. The accuracy of this method is sufficient.

It was proved that the measurement of the line capacitance per unit length C' with the accuracy of up to the second digit after comma is acceptable for most practical cases. It is not necessary to transfer the multiline TRL calibration reference impedance to $Z_{REF} = 50\ \Omega$ for extraction of the small signal model parameters, such as junction capacitances at frequencies greater than 20 GHz. This holds for the evaluated BiCMOS9MMW test chip from STMicroelectronics.

All these findings significantly simplified the requirements that have to be satisfied for the *in-situ* transfer TMR and the multiline TRL.

9 SELECTED ASPECTS OF MEASUREMENT AND CALIBRATION ASSURANCE

As it was discussed in Chapter 5, commercial standards are currently the only available reference for measuring the characteristic impedance Z_{LINE} of custom line standards above 40 GHz. Establishing the measurement assurance at the wafer level is still not completely solved. Research at NIST and later at PTB (Germany) has substantially contributed to the definition of the tractability chain at the wafer-level. Current investigations are focused on the development of robust calibration methods, uncertainty analysis as well as the design improvement for planar standards. This chapter discusses the impact of the boundary conditions and the RF probe design on the electrical characteristics of planar standards. As it is shown here, the impact of these effects is often underestimated and ignored. However, it must be taken into consideration when establishing the reference calibration at mm-wave frequencies. Furthermore, the modified ripple-test is presented as a simple practical first-order estimate of wafer-level calibration residual errors.

9.1 Optimization of Boundary Conditions for Coplanar Standards

With increasing frequency, parasitic effects caused by the environment become important, including the mechanical support on which the calibration set and the DUT are placed. They may give rise to unwanted higher-order modes and/or resonances [94, 95]. Multi-mode wave propagation on a calibration substrate is a very critical situation, since common calibration procedures assume only single-mode propagation. Any additional modes present in a system corrupt calibration and, finally, measurement data.

The line structure may not only support the desired CPW mode, but also other modes. These parasitic modes like surface-wave modes and parallel-plate modes may couple to the CPW mode beyond certain frequencies or even over the whole frequency range [96]. The critical frequencies are related to the mode order and depend on the physical dimensions of the line structure, including substrate thickness and substrate boundary conditions.

The calibration substrate should be thin enough to assure that the critical frequencies for surface mode excitation occur above the band of interest. This common solution avoids losses in propagation [97]. Unfortunately, the fundamental parallel-plate mode still can be excited and, thus, has to be considered.

The further optimization of the standard boundary conditions for mm-wave frequencies was shown in [98]. In a joint work with Ralf Doerner (FBH, Berlin) and Ed Godshalk (Maxim Integrated, USA) I developed the method of analysis and the design of experiment, did some initial measurements and calculations, planned and wrote the major part of the paper. Ralf Doerner's main contribution was in data acquisition for all experiments, extensive calculations and data post-processing. Analysis of the results was a cooperative work with Ralf Doerner and Ed Godshalk. Ed Godshalk also greatly contributed to writing and presenting the final paper.

This work was focused on distinctive boundary conditions:

1. The calibration substrate resting on a metal plate. This is a "floating ground" condition;
2. The calibration substrate resting on a material similar to the substrate material. This is a "matched" condition;
3. The calibration substrate suspended in air. This is close to an "open" condition;
4. The calibration substrate resting on radiation-absorbing material (RAM). This is a "lossy" condition (Fig. 9.1).

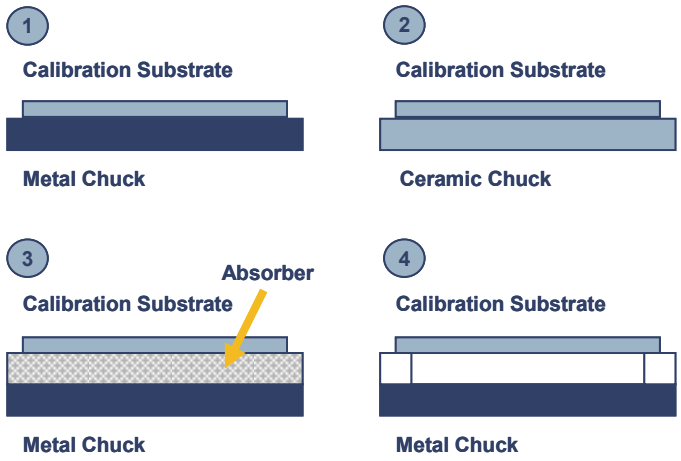


Fig. 9.1: Experimental setups providing different calibration boundary conditions: 1) Metal "grounded", 2) Ceramic "matched", 3) Absorber "lossy" and 4) Suspended "open".

The work [99] studied influences of surface-wave modes in dielectric substrates that can affect electrical characteristics of coplanar standards at mm-wave frequencies. A couple of recommendations were presented, such as suspending the calibration substrate, decreasing its thickness, and the use of radiation-absorbing materials (RAM). The practical results demonstrated noticeable improvement of the probe-tip calibration accuracy when the calibration substrate was suspended over the RAM.

Later, [97] suggested placing the calibration substrate directly on the RAM what is more practical and handy for daily use. Since then, it has become an industry-standard technique for accuracy improvement of the probe-tip calibration at mm-wave frequencies and beyond. Today, advanced RF probe systems include a calibration auxiliary chuck made from RAM [100, 101].

When measurement frequencies reached sub-millimeter wave bands, the substrate thickness could not be reduced further without the risk of damaging it during handling. For this reason, [98] investigated the approach of placing the calibration substrate on an extremely thick (compared to its own thickness, i.e. about 10 mm) ceramic support. It was shown, that the coupling between the CPW and surface wave modes can be reduced when using small enough CPW dimensions such as recommended in [99]. Experimental results invalidate the initial concern that CPW transmission lines on such a thick "substrate" would suffer from the coupling into the numerous possible modes. Nowadays, this solution is implemented in mm-wave and sub-THz probe systems (Fig. 9.2), [102, 103].

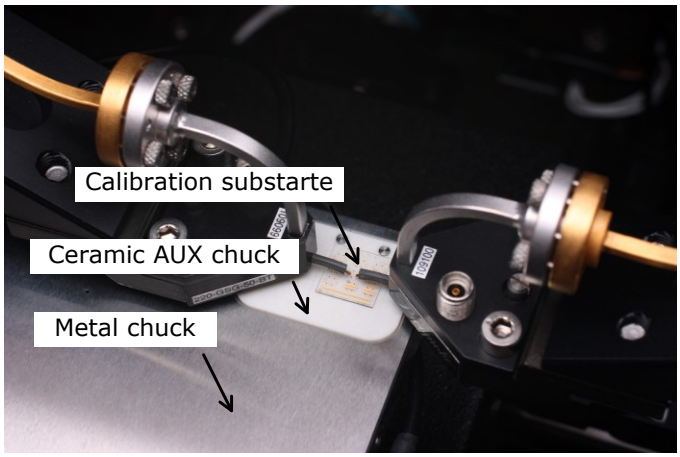


Fig. 9.2: Auxiliary chuck made of ceramic. Picture is courtesy of FBH.

Next, I show how boundary conditions influence electrical characteristics of calibration structures on a 250 µm thick calibration substrate ISS 104-783A. The results were obtained using Infinity I110-A-GSG-100 GSG probes with 100 µm pitch. Both calibration substrate and probe are from Cascade Microtech.

9.1.1 CPW Transmission Line Parameters

Propagation constant γ and characteristic impedance Z_{LINE} of a line are important figures of merit for distributed calibration standards. The propagation constant γ is extracted directly from the measurement set of lines by using the multiline TRL calibration method. The line capacitance per unit length C' is extracted from the lumped-load method allowing the determination of the Z_{LINE} from [22, 73].

The experiment was carried out for four boundary conditions (Fig. 9.1). Additionally, the parameters of the tested line were calculated according to the analytical CPW model from [104].

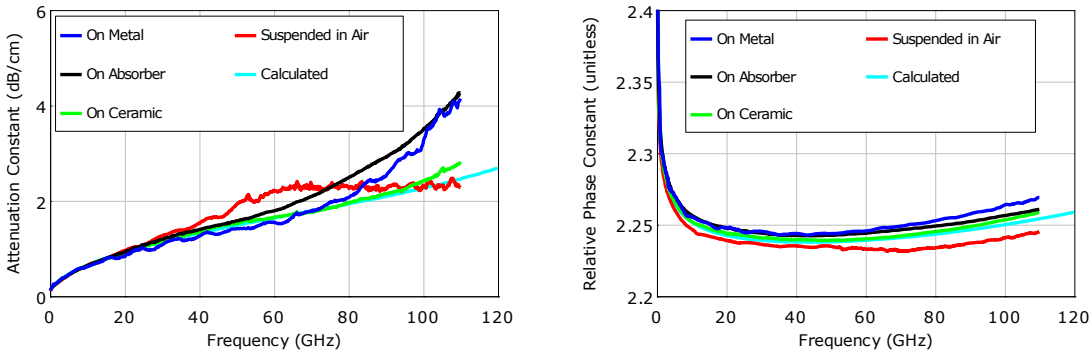


Fig. 9.3: Extracted attenuation and relative phase constants of the same CPW line from a 250 µm alumina calibration substrate for four measurement boundary conditions: direct on the metal chuck (Grounded), on metal chuck and absorber (Lossy), suspended in air (Open), and on ceramic chuck (Matched) in comparison to a model.

Results showed a noticeable impact of boundary conditions on the propagation constant γ. It should be emphasized, that the propagation constant γ was extracted under the assumption of single-mode propagation. The non-ideal behavior of the propagation constant could be attributed to a possible multi-mode propagation. Consequently, the propagation constant γ and the deduced characteristic impedance Z_{LINE} of the line differ from the case of the pure CPW mode. The "grounded" case shows a periodic ripple above 20 GHz. In contrast to this, the attenuation constant for the "lossy" case is "smoother", but beyond 60 GHz it rises faster than expected. Owing to its erratic behavior the "open" boundary is not a viable alternative above 50 GHz. The CPW line on the "matched" ceramic chuck gives the lowest attenuation and a monotonic response up to 110 GHz.

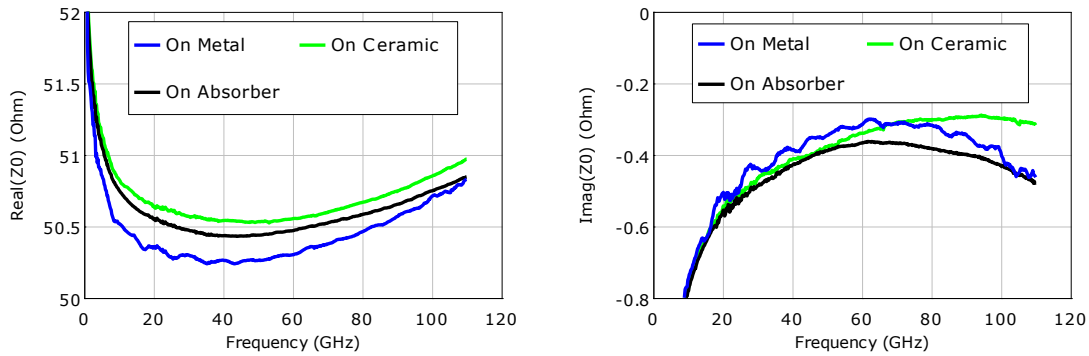


Fig. 9.4: The extracted characteristic impedance of the same CPW line from a 250 µm alumina calibration substrate for three measurement boundary conditions: direct on the metal chuck (Grounded), on metal chuck and absorber (Lossy), and on ceramic chuck (Matched).

Fig. 9.3 and Fig. 9.4 show that the "lossy" boundary leads to a strong increase of the attenuation constant and roll-off of the imaginary part of Z_{LINE} at higher frequencies.

The "matched" boundary maintains the least reactance Z_{LINE} above 85 GHz [98]. In result, the calibration and measurement accuracy is improved.

9.1.2 *Properties of Lumped Standards*

The reflection coefficient of the short element implemented on the same calibration substrate was measured with respect to the probe-tip multiline TRL. A bare ceramic area of the substrate surface was used to simulate the open standard, which was originally missing on the test substrate. The reflection coefficients of both the short and the "open-on-ceramic" element are presented in Fig. 9.5 and Fig. 9.6. Similar as for lines, it was found that the boundary conditions influence characteristics of the lumped standards already above 30 GHz.

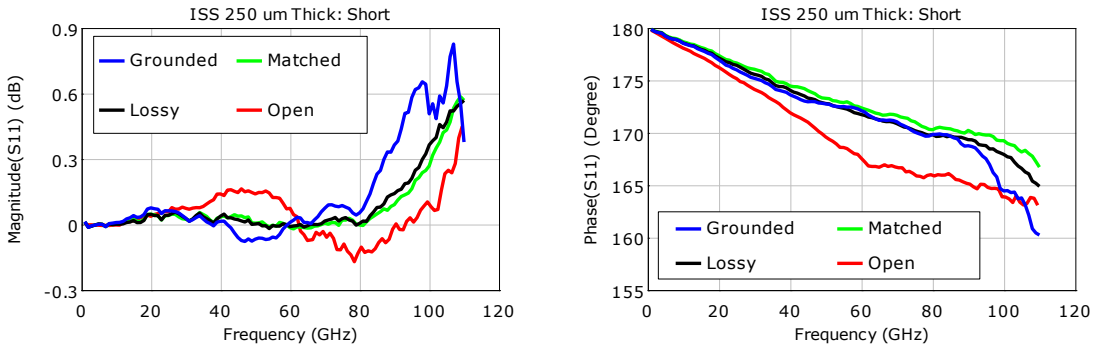


Fig. 9.5: Magnitude (left) and phase (right) of the reflection coefficient of a short on a 250 µm alumina calibration substrate, measured with respect to the multiline TRL for different measurement boundary conditions: direct on the metal chuck (Grounded), on metal chuck and absorber (Lossy), on the ceramic chuck (Matched) and elevated in air (Open).

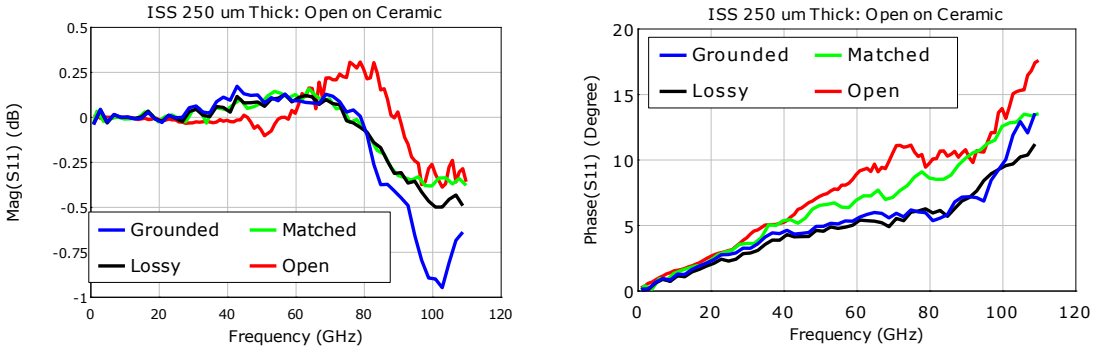


Fig. 9.6: Magnitude (left) and phase (right) of the reflection coefficient of an "open-on-ceramic" on a 250 µm alumina calibration substrate, measured with respect to the multiline TRL for different measurement boundary conditions: direct on the metal chuck (Grounded), on metal chuck and absorber (Lossy), on the ceramic chuck (Matched) and elevated in air (Open).

9.2 Impact of the Probe-Tip Design

When experimenting with boundary conditions for the calibration substrate, a fairly unexpected phenomenon was observed. The reflection coefficients of the same short and open elements corrected by the same calibration method and under identical boundary conditions differed slightly on two measurement systems. The deviations noticeably increased with frequency.

It was ensured that the calibration reference plane was accurately set to the probe tip end. Thus, applying the benchmarking multiline TRL algorithm from NIST, should exclude any differences between setups, such as probes, cables, connectors, etc. After repeating the measurements several times it was realized that the measurement errors were of systematic nature and caused by the wafer probes. In fact, one setup was equipped with Infinity Probe, while another one had ACP probes. After changing probes, it became possible to verify the original hypothesis: the residual calibration errors are also depended on the probe geometry.

The probe-to-probe crosstalk measured on a pair of coplanar shorts with a spacing of 150 µm is shown in Fig. 9.7. For this experiment the boundary conditions were “matched” by placing the substrate on an about 10 mm thick ceramic holder. Four different designs of 110 GHz 100 µm pitch GSG probes were evaluated. The system was calibrated every time by the multiline TRL.

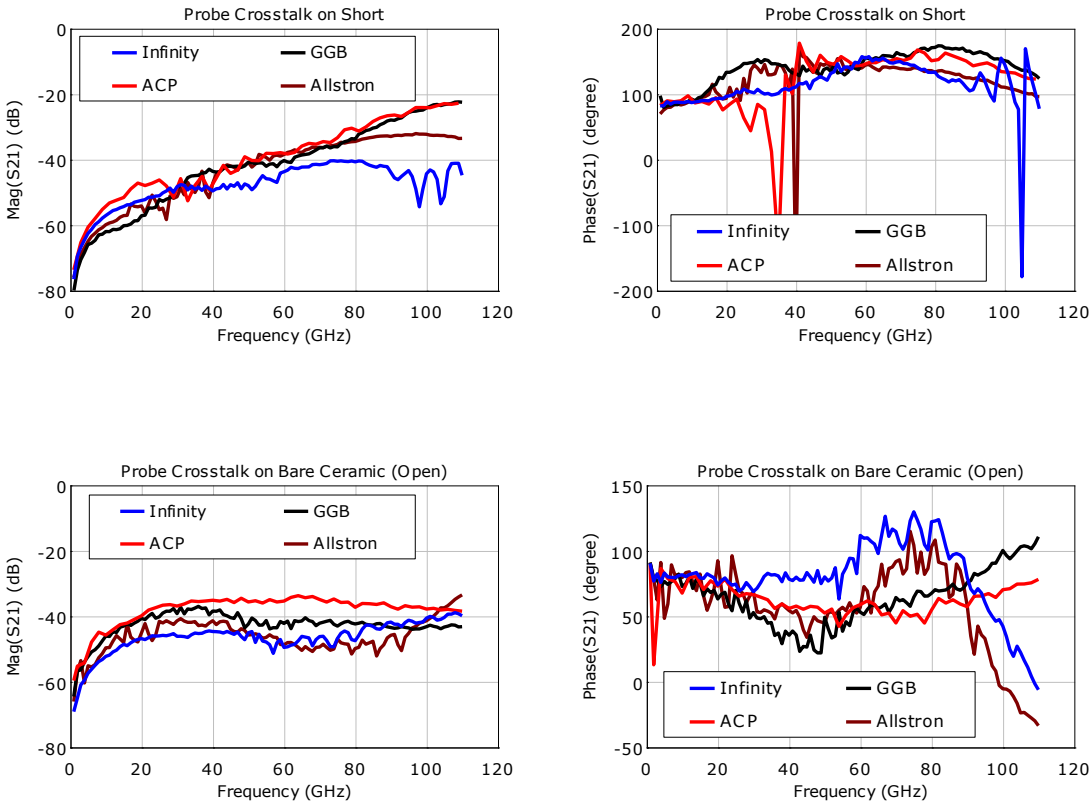


Fig. 9.7: Magnitude (left) and phase of crosstalk measured for a pair of shorts on the same calibration substrate on the ceramic chuck (Matched) corrected by the multiline TRL.

Despite the relatively simple test structure and the wide separation between the elements, the crosstalk had a more complex nature than expected. Distinct discontinuities and resonances were found in the range from 18 GHz to 50 GHz for coplanar probe types and above 80 GHz for the thin-film microstrip probe. A similar situation was observed for the “open-on-ceramic” reflection element, when probes touch a bare ceramic area on the calibration substrate.

The magnitude of the reflection coefficient of the short differs by more than 1 dB above 100 GHz (Fig. 9.8). It is obvious that extracting the equivalent circuit parameters of a DUT becomes a very hard task under such conditions. Similar to the magnitude, the phase of the reflection coefficient shows ripples and different trends. Results for the open element reveal a similar effect (Fig. 9.9).

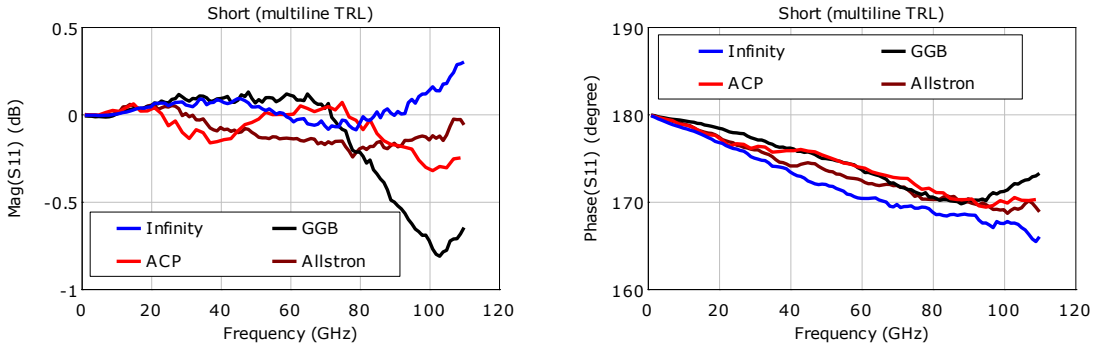


Fig. 9.8: Magnitude (left) and phase (right) of the reflection coefficients of the short on the calibration substrate on the ceramic chuck (Matched) corrected by multiline TRL.

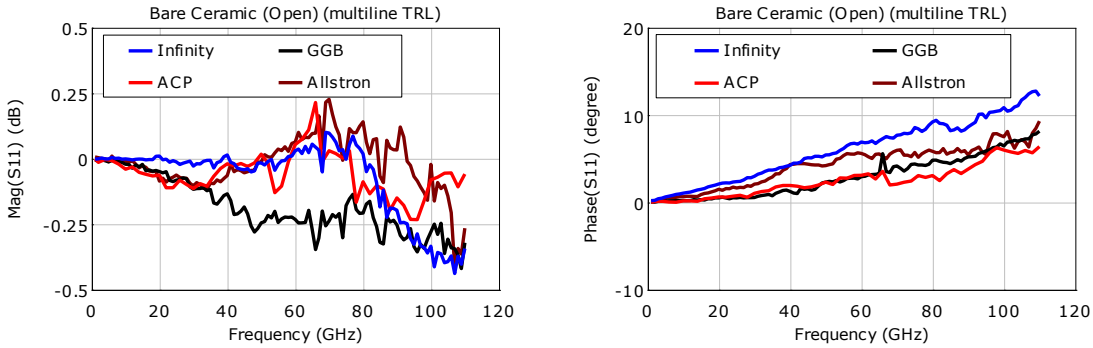


Fig. 9.9: Magnitude (left) and phase (right) of the reflection coefficients of the probes contacting a bare ceramic (open) of the calibration substrate on placed on the ceramic chuck (Matched conditions) corrected by multiline TRL.

The nature of probe-dependent residual errors is complex and still not absolutely clear. The transition of the electro-magnetic fields via the probe to the DUT is not ideal and varies depending on the probe design. Conventional calibration methods cannot

adequately address such parasitic phenomena as signal radiation, conversion to the higher-order modes, and coupling (probe-to-probe, probe-to-DUT, probe-to-chuck).

To prove this hypothesis, a similar experiment was performed in different environment and with a custom designed test chip realized on a SeGe:C process from IHP Microelectronics. The calibration standards were laid out as microstrip elements of completely different to the commercial CPW elements geometries. However, the same kind of the probe dependent calibration residual errors was identified (Fig. 9.10), [105]. Thus, the probe design indeed contributes to the calibration residual errors independent of the calibration standard design.

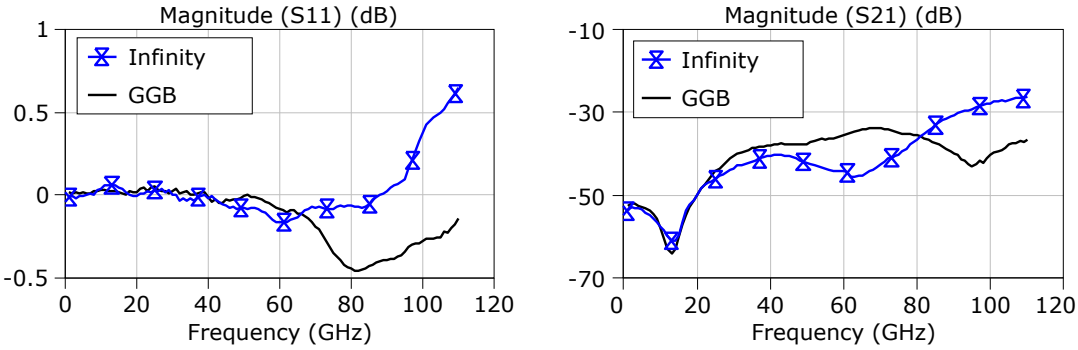


Fig. 9.10: Magnitude of the reflection (left) and the transmission coefficients (right) of the short element measured by two different RF probes. The short is design as a microstrip element and is realized as a SiGe:C test chip. Results are corrected by the TRL performed on the microstrip lines on a custom SeGe:C test chip.

Obviously, the presented results are just phenomenological. A detailed investigation, more experiments (both practical and simulation) are required to develop a good understanding of the parasitic effects discussed here. This might be an important topic for future work.

Because the discussed phenomenon was seen at nearly every stage of this work on the *in-situ* calibration, the following rules were kept across all experiments:

1. Always use probes of the same design when comparing data from different setups;
2. Place the commercial calibration substrates on a thick ceramic holder.

These rules helped me to minimize possible sources of calibration residual errors in my experiments.

9.3 Estimation of Calibration Residual Errors

A simple practical method of estimation of the calibration residual error over "ripple test" is widely used for coaxial VNA measurements. The method is based on measurement of a precision air-line that is terminated with a highly-reflective short standard at its end (e.g. [106, 107]). This configuration allows direct measurement of an effective source match, that contributes the most to the residual errors according to [108].

When measuring the residual source match, the operator estimates the maximum magnitude of ripples that appears on the reflection coefficient curve (Fig. 9.11). The effective port match is then calculated from the ripple magnitude value (or can be found in a reference table) [107]. For the given example, the ripple magnitude of 0.9 dB corresponds to the minus 26 dB source match.

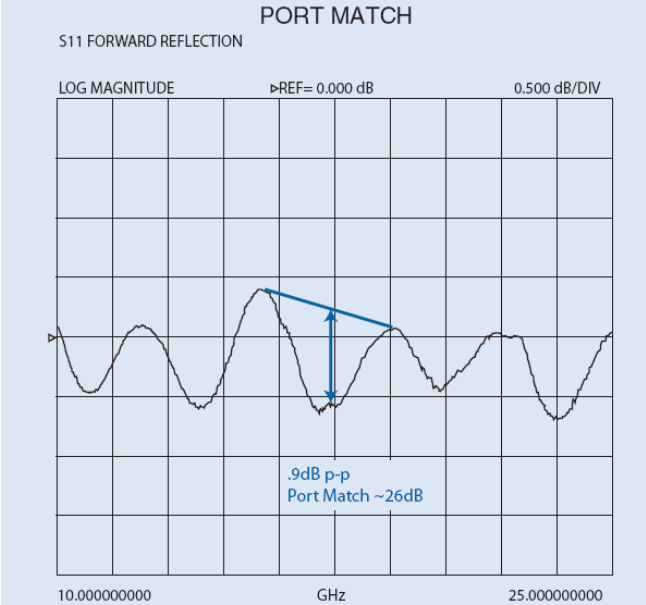


Fig. 9.11: Measuring of a port match with a conventional ripple test. Picture form [107].

The conventional procedure for measurement of the port match is a manual process that requires the operator to interact with the measurement system. A more efficient way for an automated port match measurements was proposed in [108]. However, it is not applicable for wafer-level calibration: the automated calculation procedure requires the reference line to be perfectly matched with the system reference impedance.

Together with Prof. Holger Heuermann (FH Aachen, Germany), I developed a special algorithm of an automated ripple test for wafer-level applications. The algorithm was presented in [109] (Attachment 18). In this work, I provided a list of requirements, planned the work, and made all measurements. I also calculated electrical characteristics of the reference coplanar line required for the algorithm. Prof. Heuermann implemented the impedance transformation step into the automated

ripple test, did all calculations and wrote the major part of the paper. I presented this work at the ARFTG-69th conference. The new algorithm is also described in patent applications [110, 111]. I was in charge for implementing it into the commercial calibration software SussCal Professional. This method and the software tool allowed a simple and automated estimation of the S-parameter magnitude and the phase error bounds at the wafer-level.

9.4 Conclusion

In this chapter, the boundary conditions of CPW standards and the design of the wafer probes were presented as important aspects that influence calibration and measurement accuracy at the wafer level. Before this work, these two aspects were out of scope of the research work on the establishing the wafer-level measurement assurance. It was demonstrated that they should be taken into consideration in the same manner as the variation of standard geometries and capabilities of calibration methods.

It was shown that using a thick ceramic support of the commercial calibration substrates is a preferable system configuration for measuring at mm-wave frequencies. For the novel concept probe system chuck optimized for mm-wave measurements, the US patent US7,999,563 was awarded [112]. The chuck is implemented in some advanced RF wafer-level measurement systems.

The probes of the same design were used for measurement experiments when possible. It minimized the potential impact of the probe tip design on the measurement results obtained from different system setups. Developing an explicit solution for this problem was out of the scope of this work.

A modified ripple test was developed for simple and automated evaluation of the calibration and measurement errors at the wafer level. This new method was implemented in the commercial calibration software SussCal Professional and it is protected by pending international patent applications.

10 CONCLUSION AND FURTHER RESEARCH

10.1 Conclusion

Presently, calibrating the wafer-level S-parameter system for characterization of advanced silicon devices consists of two steps. First, the system is calibrated using the commercially available calibration standards and the measurement reference plane is set at the probe tips. Next, the pad de-embedding calculates out the parasitic impedances associated with the device contact pads, the access lines, and the via stack. This approach has several drawbacks, such as limited accuracy and its complexity that increases with the frequency.

This work proposed an alternative way to calibrate the system using *in-situ* standards. The method presented here makes the intermediate probe tip calibration step obsolete. The measurement reference plane can be set close to the terminals of a lateral device. Thus, the largest portion of the contact pads and the BEOL parasitics is included into the systematic measurement error model and is eliminated by the conventional S-parameter error correction procedure. In result, the measurement accuracy is significantly improved while the system calibration procedure is simplified. The developed method enables accurate parameter extraction of advanced CMOS and BiCMOS devices at mm-wave frequencies. It appears to be a promising candidate for application at the sub-mm-wave frequency range.

The developed technique was implemented and verified on two BiCMOS and one RF CMOS processes from leading semiconductor manufactures. The experiments were carried out up to 110 GHz for all processes. The measurement frequency was solely limited by the capability of the test equipment. The verification results demonstrated that the new technique significantly outperformed the conventional method in measurement accuracy already from 20 GHz. It was also demonstrated that the accuracy of the conventional method can be increased by implementing complex de-embedding methods, such as the scalable six-step procedure. However, the new *in-situ* calibration developed in this work wins over the advanced de-embedding methods thanks to its ease of implementation.

The key contribution of this work was to realize the lumped-standard based transfer TMR calibration method on silicon. The main advantage of such a method over the distributed-standard based calibration methods (such as TRL and the multiline TRL) is that all standards take relatively little space on the test chip and share the same geometry. Therefore, the transfer TMR has two significant advantages over TRL-like methods:

1. Saving expensive space of the test chip: for both CMOS and BiCMOS implementations, the transfer TMR standards required about 15 times less of the test chip size than the multiline TRL standards;
2. Repositioning of the wafer probes during the calibration process not required: calibration can be easily automated, increasing the repeatability while reducing the calibration time, and, finally, the calibration costs.

Previously, there were several attempts to implement the *in-situ* lumped-standard calibration on silicon (e.g. [71]). Since then, it has become a common understanding in industry that it was generally difficult to replace the pad de-embedding step by the straightforward *in-situ* calibration for silicon processes. In particular, the application of conventional lumped-standard calibration methods (such as SOLT) on silicon is very challenging and, therefore, is considered to be worthless. By adopting the transfer TMR, this work opened new perspectives on how to improve the accuracy of the system calibration and the device characterization. It enabled accurate device parameter extraction and model verification at upper mm-wave frequency bands.

Based on a detailed analysis, this work proposed an optimal solution for each step of the development, implementation, and verification of the *in-situ* calibration. That included the analysis of the capability of modern VNAs, the development and validation of calibration solutions suitable for silicon applications, the location of the *in-situ* calibration and the measurement reference plane, the creation of generalized calibration standard design rules for both CMOS and BiCMOS technologies, the characterization of calibration standards, and, finally the verification of calibration and measurement accuracy.

The transfer TMR (commercial name: LRM+) and the general RRMT+ developed in this work were implemented in the wafer-level calibration software SussCal Professional from SUSS MicroTec (later WinCal 4.5 from Cascade Microtech). Three patents have been granted and four patent applications were filed for methods and techniques presented here.

10.2 Further Research

Going beyond the original scope of this work, some aspects of the *in-situ* calibration technique could be subject to additional research. It particularly concerns such topics as the calibration over multiple temperatures, multiport calibration, solutions for systems affected by a strong port crosstalk and the multimode signal propagation, as well as establishing *in-situ* calibration and measurement assurance.

10.2.1 Calibration over Multiple Temperatures

Modeling, parameter extraction, and model verification require several measurement series of the same DUT at multiple temperatures. The DUT has to be heated up or

cooled down in a wide temperature range (at least from minus 40°C to plus 125°C) to characterize the variation of its temperature-dependent parameters. A similar dependency is to expect for the electrical properties of the *in-situ* calibration standards and has to be taken into account. Chapter 8 presented a method to analyze and improve the over-temperature calibration accuracy. For reason of generalization, all investigations were carried out on commercially available ceramic calibration substrates. It was shown, that the variation of the load resistance with the measurement temperature is the most influencing factor on the accuracy of the lumped-standard based calibration. While a similar constellation is highly probable to expect for the *in-situ* calibration, an experimental prove of this hypothesis is still outstanding. Also, the characteristic impedance Z_{LINE} and the propagation constant γ of the thru standard may differ in their variation over temperature depending on the design of standards, process specifics, and the frequency range.

10.2.2 Multiport Calibration

As discussed in Chapter 3, some advanced device characterization techniques as well as the IC design verification demand a multiport *in-situ* calibration solution. The general multiport RRMT+ method was developed and verified to address these challenges. It was proved that the RRMT+ has significant advantages over conventional methods: it enables the use of not-ideal reflect and asymmetrical load standards. In addition, RRMT+ relaxes requirements to the cross-over and the loop-pack thru standards that are very hard to characterize and to realize on a test chip. This work proved capabilities of the RRMT+ method up to 40 GHz on a commercial ceramic calibration substrate. As RRMT+ is a further development of the transfer TMR algorithm, their design requirements to the *in-situ* standards mostly resemble each other. The verification of the RRMT+ on a specific silicon process is the subject of future investigations.

10.2.3 Solution for Multimode Propagation Conditions

This work revealed some specific aspects of mm-wave on-wafer calibration and measurements that may require a special attention. It became obvious that the design of the RF probe tip contributes to calibration residual errors at mm-wave frequency range. This effect can be explained by unwanted probe coupling with the test structure, the excitation and propagation of higher order modes, and the signal radiation. These factors should be taken into consideration when expanding the proposed method to sub-THz frequencies. All efforts must be taken to prevent (or to suppress) propagating of the higher order modes in calibration standards. However, this might become difficult to realize. Alternatively, the systematic error term model can be extended to address the multimode measurement conditions. This will require a corresponding multimode calibration solution, which is not present at the moment.

10.2.4 Crosstalk

The evaluated multiline TRL and the transfer TMR calibration methods are based on the commonly used seven-term model of systematic measurement errors. Therefore, the final error correction of the DUT S-parameters is provided by the test instrument. The device characterization software can download error-corrected DUT S-parameters from the VNA memory and perform further data processing (de-embedding, parameter extraction, etc.). This is a significant advantage, because the management of big arrays of the error terms is under the responsibility of the VNA firmware. However, the seven-term model does not address the crosstalk between the between the device terminals. Further improvement of the proposed *in-situ* calibration method may be done by including the port crosstalk terms into the error model. This will lead to a more complex calibration solution, but will support measurements close to THz frequencies. Most important, however, is that the optimization and the implementation steps of such advanced methods will remain similar to those presented in this work.

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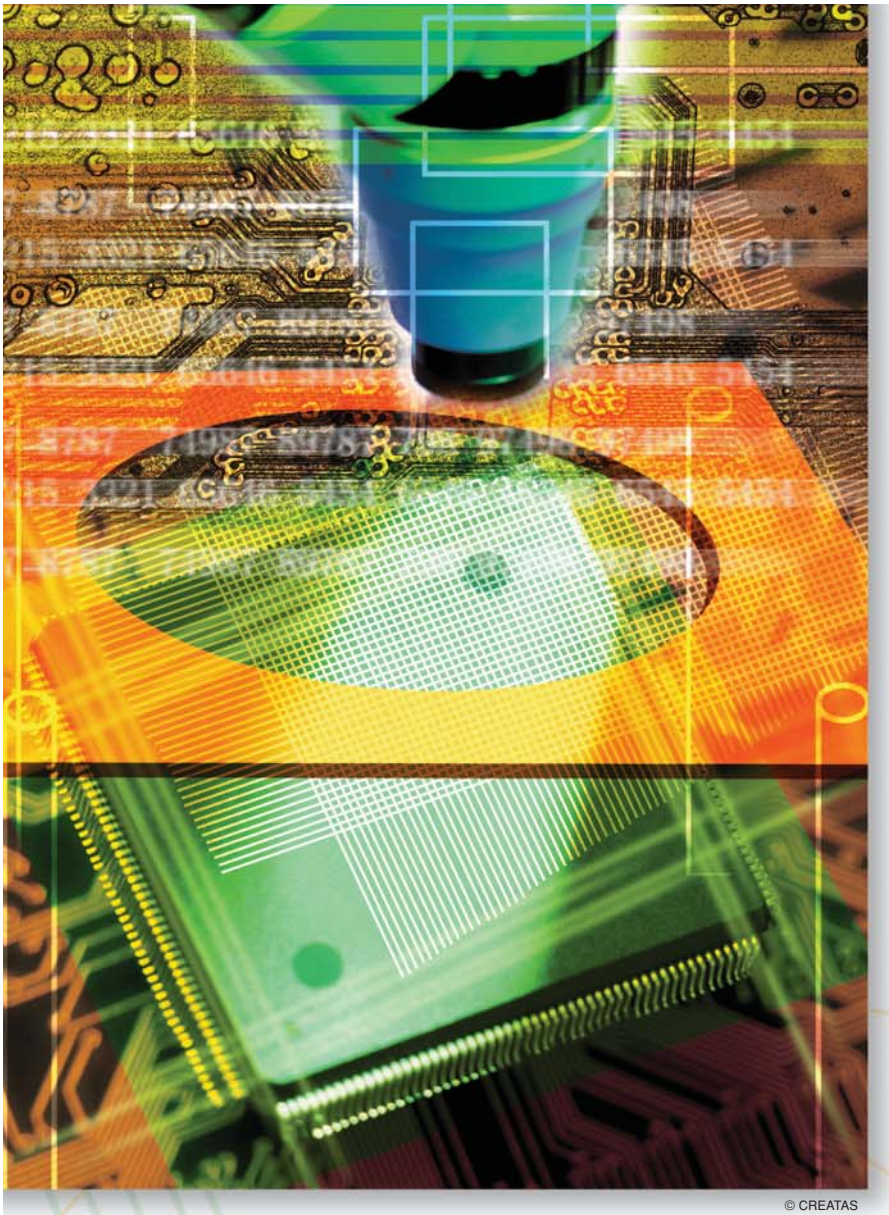
12 ATTACHMENT TO CHAPTER 2

12.1 Paper [32]: “VNA Calibration”

A. Rumiantsev and N. Ridler, "VNA calibration," *Microwave Magazine, IEEE*, vol. 9, pp. 86-99, 2008.

In this paper, I presented a detailed investigation of the history and the state-of-the-art of VNA measurements and S-parameter calibration techniques. My co-author, Nick Ridler from National Physical Laboratory (NPL, UK) added metrological aspects to this paper, such as the definition of measurement traceability, measurement assurance as well as clarification of the term “calibration” that, in fact, has multiple meanings for vector network analysis. This research helped to form a strategy of how to approach the specific problem of the on-wafer calibration on silicon.



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VNA Calibration

Andrej Rumiantsev and Nick Ridler

It was during the late 1950s that the need for reliable measurement, and therefore reliable measurement standards, at RF and microwave frequencies began to emerge. This led to the introduction of precision coaxial air lines as primary reference standards of impedance [1], [2]; see Figure 1. These lines use conductors made from very-high-conductivity metals and air as the dielectric, due to the simple and predictable electromagnetic properties (i.e., permeability and permittivity) of air at RF and microwave frequencies [3]. This ensured that the properties of these lines were very close to those of ideal lines [4].

Also during the late 1950s and throughout the 1960s, much work was undertaken to develop precision coaxial connectors to ensure that very repeatable and reproducible measurements could be made at microwave frequencies [5], [6]. To help focus this effort, committees were established (including an IEEE subcommittee on precision coaxial connectors [7]) tasked with producing standards for these precision connectors. Finally, by the late 1960s, the first fully automated vector network analyzers (VNAs) providing high-precision measurement capabilities were introduced (e.g., [8], [9]). The stage was now set for work to begin on introducing reliable measurement assurance techniques for measurements made using VNAs (Figure 2).

However, there were several other key developments that took place during the 1970s, 1980s, and 1990s that greatly improved the state of the art of measurements made using VNAs. These included the introduction of:

- smaller precision coaxial connectors (beginning with the 3.5-mm connector [10] and ending with the 1-mm connector [11]), enabling measurements to be made over wider bandwidths
- VNA calibration and verification kits containing high-precision devices suitable for calibrating and/or verifying the performance of the VNAs
- reliable VNA calibration techniques [including thru-reflect-line (TRL) [12], line-reflect-line (LRL) [13], etc.)

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- six-port VNAs [14] used by national measurement standards laboratories [such as the National Institute of Standards and Technology (NIST) in the United States and the National Physical Laboratory (NPL) in the United Kingdom, etc.] to provide an independent measurement method to verify the performance of the commercially available VNAs.

Finally, also by the late 1980s and early 1990s, national measurement standards laboratories (i.e., NIST, NPL, etc.) began turning their attention to demonstrating the reliability of VNA measurements made on planar circuits (such as on-wafer measurements) to support the rapidly developing microelectronics industry. Both NIST and NPL produced standard wafers [15], [16] that contained the planar circuit equivalent to the coaxial air line—i.e., precision sections of coplanar waveguide and/or microstrip transmission line. These lines provided the reference standards for calibrating VNAs for on-wafer measurements.

All of the above activities greatly improved the state of the art for practitioners and users of VNA measurements. Also, in addition to all these activities, much was done by measurement experts working in industrial, academic, and government laboratories to establish traceability and other quality assurance mechanisms for these VNA measurements. These topics are discussed in "What is Traceability?" and "Measurement Assurance."

Systematic Measurement Errors

What Is Calibration and Error Correction?

Calibration is defined as the "set of operations that establish, under specified conditions, the relationship between values of quantities indicated by a measuring instrument or measuring system, or values represented by a material measure or a reference material, and the corresponding values realized by standards" [17]. As such, calibration traditionally involves having an instrument or component sent away periodically to a standards and/or calibration laboratory, who then undertake the calibration process. This often results in a certificate of calibration being issued that demonstrates the current condition of the instrument or component.

However, in the context of a VNA, the term calibration can have at least two different meanings. First, the traditional concept of calibration can still be applied, with the VNA being sent away for calibration, typically every year or so. (Alternatively, some companies offer periodic on-site calibration, performed by a visiting calibration specialist.) However, of more relevance to this article is another form of calibration that is performed locally, usually each time the instrument is set up and configured for a given series of measurements. This second form of calibration is intended to remove systematic errors from the instrument hardware (and to take into account the presence of any accessories that may have been added to enable specific measurements to be performed) at the required frequencies for the measurements. For example, measurements may be required to be made in an on-wafer environment. In which case, first cables need to be connected to the VNA front-panel connectors, followed by coaxial adaptors, and finally on-wafer probes (Figure 3). This second form of calibration will correct for the effects of these added components as well as correct the systematic errors in the VNA. This is why this type of calibration is often referred to as *error correction*, and it is this type of calibration that will be discussed in this article.

The demand for increased measurement accuracy from the VNA can be achieved by improving the hardware, the models used for characterizing measurement errors, the calibration methods used for calculating these errors, and the definitions of calibration standards. For *S*-parameters, the systematic errors are often represented using so-called error models of the measurement system (i.e., VNA). The number of error coefficients included in the error model, as well as the type of error model, depends on

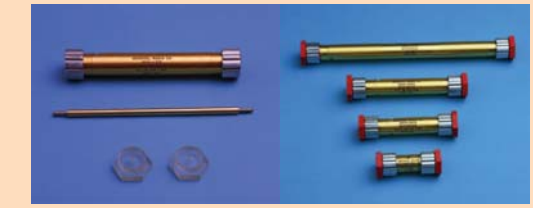


Figure 1. *An example of precision reference coaxial air lines of different length.*

Figure 2. *A coaxial mm-wave measurement bench based on the Agilent 8510 VNA. This analyzer was the industry reference for microwave measurements for many years.*

What Is Traceability?

Traceability, in the context of a measurement, is defined as the "property of the result of a measurement or the value of a standard whereby it can be related to stated references, usually national or international standards, through an unbroken chain of comparisons all having stated uncertainties" [17]. Applying this concept to a VNA measurement, the stated references could be precision air lines (or their equivalent), the VNA is the transfer device used as part of the unbroken chain of comparisons, and the precision connectors enabling these comparisons to be made within acceptable limits to the uncertainty of measurement.

The benefit of having a measurement that is traceable stems from the fact that it can be used to demonstrate the equivalence of measurements made independently of one another. This is of paramount importance in a customer/supplier relationship where a common understanding is needed of the parameters that define (or specify) the performance of the device being bought or sold. Therefore, if two measurements of a quantity are made independently, and these measurements are both traceable, then their values will agree to within the stated uncertainties of the measurements. This is, therefore, an extremely valuable process that can provide the necessary underpinning assurance that is needed when operating within a truly global marketplace where the customer and supplier may be located in different parts of the world.

The vital role that traceability can play was recognized long ago and led to the introduction of national measurement accreditation schemes so that customers and suppliers could fully demonstrate the quality of their measurements to an independent third party (i.e., the accreditation body). These days, such accreditation processes are controlled by international standards (e.g., [72]), thus ensuring that the accreditation process is itself applied uniformly across all types of measurements and at all locations around the world. Most countries maintain a national accreditation body for this purpose, and these bodies are themselves linked through international accreditation organizations such as the International Laboratory Accreditation Cooperation (ILAC, www.ilac.org).

When traceability is harmonized within an agreed system of units (e.g., the international system of units, SI), then not only is it possible to demonstrate equivalence between measurements of the same quantity, but it also becomes possible to demonstrate the equivalence of measurements of different quantities. This is achieved through the relationship of these quantities to the so-called base quantities within the system of units. (In SI, the seven base quantities are length, mass, time, electric current, thermodynamic temperature, amount of substance, and luminous intensity.)

By following the traceability path of a measurement back to its fundamental base quantities, it is possible to demonstrate the harmonization of the measurement within the system of units. For example, a reflection measurement made along a transmission line can usually be traced back to dimensional measurements, since it is the dimensions of the transmission line that determine the impedance and therefore the amount of signal that is reflected by the line. The base quantity for dimensional measurements is length. Similarly, for power and noise measurements, these can usually be related back to heating effects. Therefore, the base quantity is thermodynamic temperature. In just about all microwave measurements, the frequency of the measurement needs to be known. Since frequency is the reciprocal of periodic time, the base quantity is time.

A key role of a national measurement standards laboratory (such as NIST, NPL, etc.) is to maintain primary reference standards of measurement. For example, at microwave frequencies, these are usually standards of power, impedance, attenuation, noise, etc. In addition, the national measurement standards laboratory is tasked with realizing the seven SI base quantities. By linking these two roles, the national measurement standards laboratory is able to deliver a wide range of traceable measurements to industry that are also harmonized within the SI.

The subsequent 'linking' of the capabilities of one national measurement standards laboratory to others is achieved through participation in international measurement comparison programs conducted under the auspices of organizations such as the International Bureau of Weights and Measures (BIPM, www.bipm.org) and their consultative committees. The results from these comparison exercises are analyzed and placed on a database maintained by the BIPM that demonstrates the capability of each national laboratory.

Finally, it is worth mentioning that these days, with the global accessibility of the Internet, measurement services that make extensive use of the Internet are beginning to be developed. These services are starting to play a role in providing traceable measurements in a highly efficient manner. For example, a system has recently been put in place by NPL that uses the Internet to provide traceability for high-precision measurements using VNAs at any location around the world [73].

- the hardware topology of the VNA,
- the number of VNA ports and measurement receivers
- the required measurement accuracy.

The following section presents commonly used models of *S*-parameter systematic measurement errors.

Flow-Graph S-Parameter Representation

The first error models used for automated S-parameter error correction were introduced at the end of the 1960s. They addressed the bidirectional two-port system and defined the influence of system imperfection on reflection (S_{11}, S_{22}) and transmission (S_{21}, S_{21}) measurements. These models were developed to represent systematic measurement errors using imaginary two-port error networks. They were described by S-parameters and were included in the measurement signal paths [8]. The model for a reflection (one-port) measurement consisted of only one error network. Originally, this network was described as a matrix of four *S*-parameters.

Measurement Assurance

Although traceability provides arguably the most acceptable method for assuring a given measurement, it is not always possible to provide such traceability for all types and ranges of measurement. This is particularly true of modern VNAs that offer many different measurement formats (e.g., logarithmic or linear; single-ended or differential; frequency- or time-domain; etc.) often over very wide dynamic ranges (sometimes up to 100 dB or more). Under these circumstances, the measurement community benefits from the use of additional assurance techniques to validate results from VNAs.

The first major contribution to this area was the introduction of verification standards and kits for VNAs [74], [75]. These verification kits can be measured routinely by the end-user and compared with reference values supplied by the manufacturer. The kits can also be returned periodically to the manufacturer, who checks the reference values. This provides a high degree of measurement assurance for the end-users. Verification kits have since been produced in many of the different types of connectors used by the industry, as well as in waveguide.

Another activity that has been very valuable to measurement practitioners in our industry is the user groups that have been set up over the years. These groups have enabled the key measurement issues, at any given time, to be identified, discussed, and resolved. Probably the first such user group set up by RF and microwave specialists was the Automatic RF Techniques Group (ARFTG), www.arftg.org , which was established back in 1972 [76]. ARFTG is a technical organization interested in all aspects of RF and microwave test and measurement. The group is still very active today, and continues to evolve in response to the many developing needs of the RF and microwave community. For example, a recent development within ARFTG has been the establishment of a Nonlinear Vector Network Analyser (NVNA) Users' Forum. This informal group meets three times each year - during the Spring ARFTG conference (which is itself part of Microwave Week), the Fall ARFTG Symposium, and European Microwave Week.

Other user groups of interest to the VNA community include ARMMS (www.armms.org)—the RF and Microwave Society—and ANAMET (www.npl.co.uk/anamet)—the RF and Microwave Metrology Club. Like ARFTG, these groups meet twice each year to discuss issues of relevance to each group.

An activity that some of these user groups undertakes is to provide the opportunity to participate in measurement comparison programs (MCPs). These are programs that allow many participants to make measurements of the same devices that travel between the participating laboratories [77], [78] (see Figure A). The results of the measurements of these traveling standards are compared to indicate the overall equivalence (or not) of the results. Such exercises are extremely useful for identifying serious errors that may be present in measurements made by any of the participants. Comparisons can also be undertaken in areas of measurement where traceability may not yet exist (e.g., time-domain measurements [79]).

All of the above processes—local auditing using verification kits, interactions with user groups, participation in MCPs—provide measurement assurance which complements that provided by classical traceability processes. Ultimately, for the very highest level of measurement assurance, one should consider traceability of measurement along with one or more of these other processes.

Figure A. *Type-N travelling standards used for the ARFTG MCP.*

However, it turned out that only the coefficients S_{11} and S_{22} and the product $S_{21}S_{12}$ were needed for further error correction. As a result, the three-term error model replaced the matrix consisting of four *S*-parameters where the coefficients e_{00}, e_{11}, and e_{01} are E_D (directivity), E_S (source match), and E_R (reflection tracking), respectively (Figure 4) [18]. Today, the three-term error model is still the most common representation of one-port calibration and error correction procedures.

Following from the above, the eight-term model represented the bidirectional system for automated measurements of two-port devices under test (DUTs) (Figure 5). The *S*-parameter-based model [Figure 5(a)] required all four coefficients (S_{11}, S_{12}, S_{21}, and S_{22}) to be known for each error adapter. The error correction of the transmission measurements included two factors $S_{21}^{(1)}S_{12}^{(2)}$ and $S_{21}^{(2)}S_{12}^{(1)}$ for the forward and reverse directions, respectively [8]. These factors were addressed as coefficients E_T in the error terms representation [Figure 5(b)] [19].

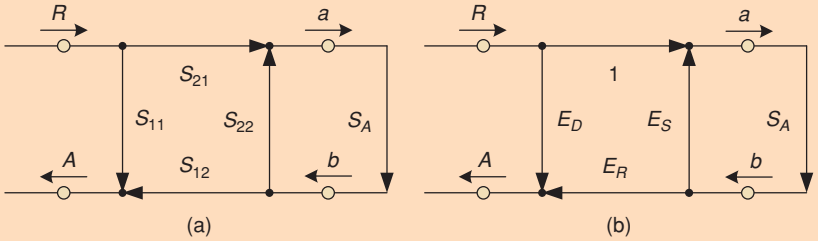
Alternative unidirectional test sets did not include an internal switch for redirecting the incident measurement signal between measurement ports. They allowed the DUT to be characterized in one direction only (for its S_{11} and S_{21} parameters). As introduced in [18], such a system can be described by only five error terms. An additional term represents the signal leakage between the measurement ports, thus extending the model to six parameters [18], [20] (see Figure 6).

The leakage terms (also called *crosstalk terms*) were later added to the eight-term model, one for each measurement direction, increasing the number of the error coefficients in general to ten [21].

The 8(10)- and 5(6)-term error models were in use for almost ten years without significant modification. [Note that here and elsewhere in the article, the number in parentheses represents the number of error terms, including any leakage terms (E_X). These terms are optional parameters that may not fully represent the crosstalk (as discussed further in this article) and thus we do not count it in our nomenclature.] Within any model, the error terms need to be defined for each measurement frequency point and saved in the VNA memory. Therefore, an extension of the error model, including the use of additional error terms, or development of a unified error model for different test sets were not commercially viable options. (At that time, the cost of computer memory was still a major design consideration.)

Rapid progress in semiconductor technologies at the end of the 1970s significantly expanded the availability of low-cost read/write memory modules as well as mass storage devices embedded in measuring instruments. This greatly extended the capabilities of VNA error modeling. The measurement system description was unified and the 10(12)-term model was introduced for commercial VNAs independent of the test set configuration [19] (see Figure 7). This error model became the standard model for the description of systematic measurement errors of a

Figure 3. *(a) An example of a state-of-the-art 300-mm RF and microwave wafer-level measurement system. The system includes: the EMI-shielded and light-tight automated probe system with integrated thermal management and automated RF calibration, a VNA, RF cables, and RF wafer probes. (b) The set of coplanar calibration standards (a calibration substrate) is used for the calibration of the system.*



The relationship between the actual S_A and the measured S_M=A/R S-parameter of the DUT is given by

$$S_{11A} = \frac{S_{11M} - E_D}{E_S(S_{11M} - E_D) + E_R}$$

Figure 4. *The one-port three-term error model in (a)* S*-Parameter and (b) error terms representation.*

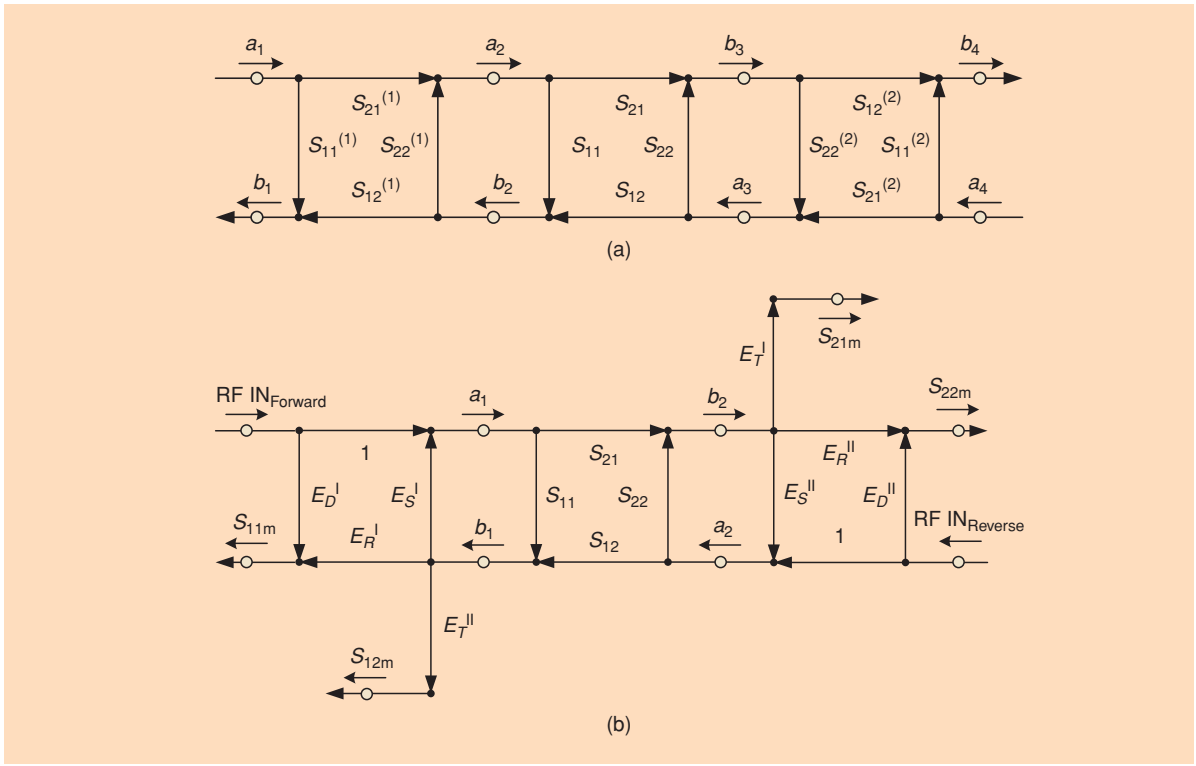


Figure 5. *The eight-term error model of a two-port VNA in (a)* S*-Parameter and (b) error terms representations. The unknown DUT* [S] *is connected between the error adapters. Prime and double-prime parameters correspond to the forward and reverse measurement directions, respectively.*

two-port VNA. It is implemented in all modern measurement instruments.

The equations for the relationship between the measured and actual *S*-parameter of a two-port DUT were given in [19] and [22]. However, these equations are somewhat bulky. An alternative simplified approach was introduced in [23]. For the measurement system, the relationship between the measured, *m*, waves and the incident, *a*, and reflected/transmitted waves, *b*, at the DUT can be found using the scattering parameter definition:

$$\begin{pmatrix} m_2^I \\ a_1^I \end{pmatrix} = \begin{pmatrix} E_D^I & E_R^I \\ 1 & E_D^I \end{pmatrix} \begin{pmatrix} m_1^I \\ b_1^I \end{pmatrix}. \tag{1}$$

From (1) and Figure 7, the incident a_1^I, a_2^I, reflected b_1^I, and transmitted b_2^I waves at the DUT are

$$\begin{aligned} a_1^I &= m_1^I + \frac{E_S^I}{E_R^I}\left(m_2^I - E_D^I m_1^I\right), \\ b_1^I &= \frac{1}{E_R^I}\left(m_2^I - E_D^I m_1^I\right), \\ b_2^I &= \frac{m_4^I}{E_T^I}, \quad a_2^I = \frac{E_L^I m_4^I}{E_T^I}. \end{aligned} \tag{2}$$

The parameters $a_1^{II}, a_2^{II}, b_1^{II}$, and b_2^{II} can be found in a similar way, taking into account the switch in its other position. Once the wave parameters *a* and *b* are defined, the following matrix can be formed:

$$\begin{pmatrix} b_1^I & b_1^{II} \\ b_2^I & b_2^{II} \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1^I & a_1^{II} \\ a_2^I & a_2^{II} \end{pmatrix}, \tag{3}$$

or, in short,

$$[K] = [Sx][L]. \tag{4}$$

Finally, the *S*-parameters of the DUT can be found by

$$[Sx] = [K][L]^{-1}. \tag{5}$$

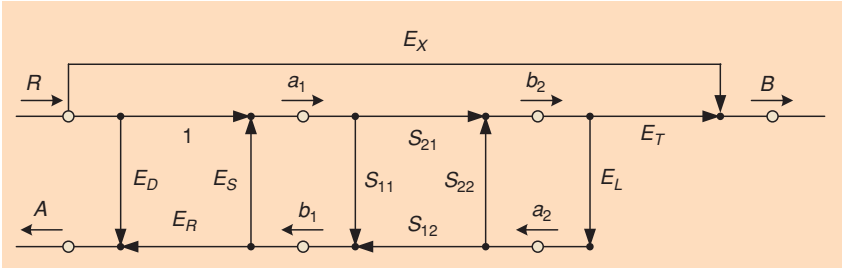


Figure 6. *The five-term unidirectional error model, represented by the error coefficients* E_D, E_S, E_R, E_L, *and* E_T. *The leakage coefficient* E_X *is an optional parameter.*

Cascade Matrix T-Parameter Representation

The ten-term model, as described above and shown in Figure 8, represents the systematic measurement errors in terms of effective *S*-parameters. A different concept was introduced by engineers from Tektronix in 1975 [24]. They proposed describing the systematic measurement errors of a two-port system as two error boxes, characterized by transmission (*T*) parameters (Figure 9). Their model included eight error terms. However, as it was later demonstrated in [12] and [25], only seven error terms are needed for further error correction. To distinguish this approach from the old *S*-parameter-based eight-term model [8], it is usually referred to as the *seven-term model*.

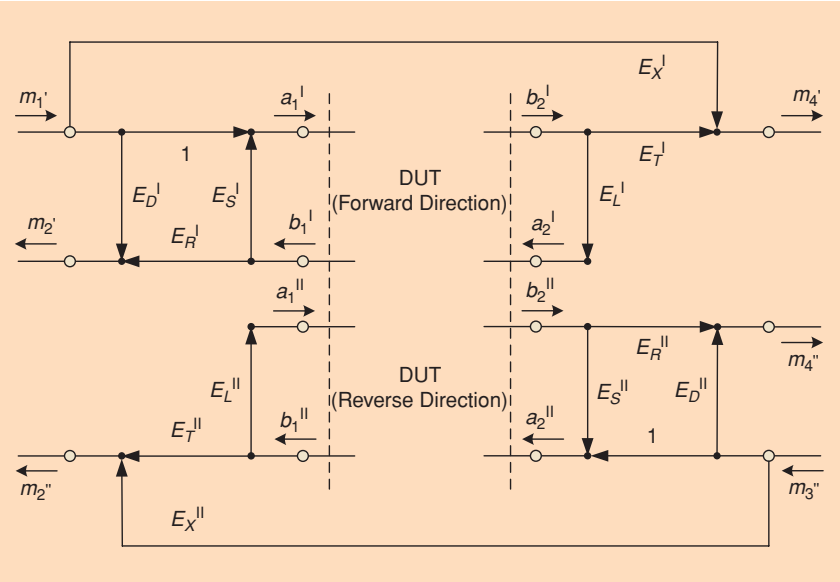


Figure 7. *The 10(12)-term error model for two-port bidirectional* S*-parameter measurements. The error coefficients* E *represent the relationship between waves,* m*, measured by the ideal VNA receivers and incident,* a*, and transmitted/reflected waves,* b*, at the DUT plane. Prime and double-prime parameters correspond to the forward and reverse measurement directions, respectively.*

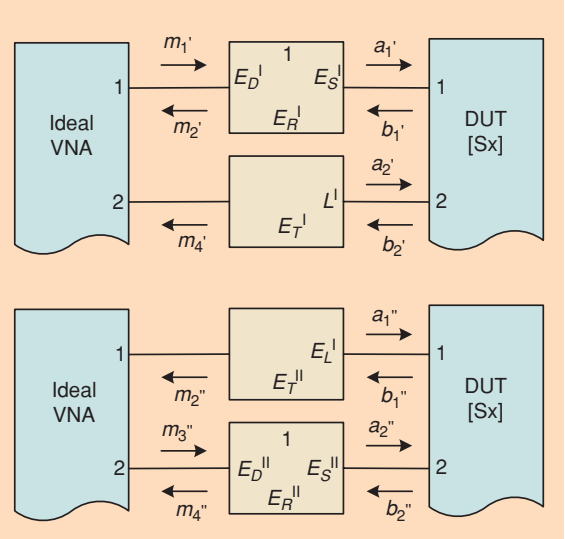


Figure 8. *Block diagram of a two-port VNA described by the ten-term model for the first and second state of the switch.*

Impact of VNA Measurement Receivers

It is common to relate the ten-term error model with the reference channel hardware concept of the VNA. The reference channel VNA has one reference receiver for detecting the incident signal and several measurement receivers, one for each VNA port. Thus, for the *n*-port system, the total number of receivers, *k*, is: $k = n + 1$, where *n* is the number of measurement ports (Figure 10).

The application of the seven-term model requires a VNA built on a so-called double-reflectometer principle: every measurement port is related with the individual reference and measurement receivers. For instance, the two-port double-reflectometer VNA uses four measurement receivers (Figure 11). In general, the number of measurement receivers *k* for a multiport double-reflectometer is $k = 2n$, where *n* is the number of system measurement ports.

Figure 11 shows a physical model of the systematic errors for a four-receiver VNA where [*Tx*] is a measured DUT and [*A*] and [*B*] are the error boxes. The latter describe measurement systematic errors. The values $m_1 \ldots m_4$ represent waves measured by ideal receivers.

It is straightforward to show that the relationship between $m_1 \ldots m_4$, incident (a_1, a_2), and reflected or transmitted (b_1, b_2) signals is:

$$\begin{pmatrix} m_1' & m_1'' \\ m_2' & m_2'' \end{pmatrix} = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \times \begin{pmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{pmatrix}^{-1} \begin{pmatrix} m_3' & m_3'' \\ m_4' & m_4'' \end{pmatrix}, \quad (6)$$

where: $m_1' \ldots m_4'$ and $m_1'' \ldots m_4''$ are the measured values in forward and reverse directions, respectively. $T_{11} \ldots T_{22}$ are defined as the transmission parameters of a measured DUT. Alternatively, in shortened form,

$$M = ATB^{-1}, \quad (7)$$

where measurement matrix *M* is

$$M = \begin{pmatrix} m_1' & m_1'' \\ m_2' & m_2'' \end{pmatrix} \begin{pmatrix} m_3' & m_3'' \\ m_4' & m_4'' \end{pmatrix}^{-1}. \quad (8)$$

Finally, the T-parameters of the DUT are given by

$$T_X = A^{-1} M_x B. \quad (9)$$

Conversion of Error Models

Both seven-term and ten-term error models are used to describe the double-reflectometer VNA. If required, a seven-term model can be converted into a ten-term model. Several approaches have been published giving different conversion equations [22], [26]–[28]. These equations are slightly different, but are based on the same physical principle. The differences stem from the authors' notation used for the seven-term model elements, e.g., using the inverse of matrix [B]. Such conversion techniques are implemented in many double-reflectometer VNAs today.

There were also attempts to apply the seven-term model for the reference receiver VNA [29]. In fact, this assumes that the source match equals the load match of the test set, which holds only in the case of an ideal test set switch. For a real system, this assumption may lead to intolerable measurement inaccuracy, especially for highly reflective DUTs [30]. Only the ten-term model can guarantee the entire description of the reference receiver VNA.

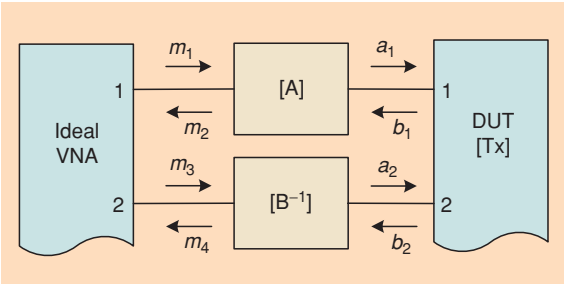


Figure 9. *Block diagram of a two-port VNA described by the cascade matrix representation (seven-term model).*

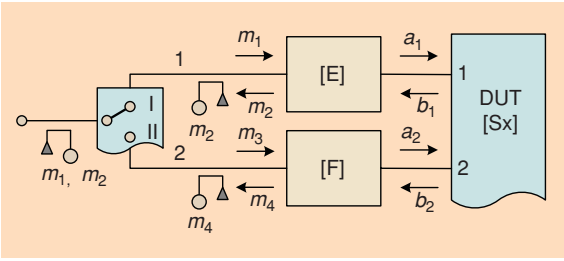


Figure 10. *Block diagram of VNA based on the reference channel architecture. It shows one reference receiver for incident signals* m_1 *and* m_3*, the signal source switch, the measurement receivers for signals* m_2 *and* m_4*, and the ten-term error model matrices* [E] *and* [F].

Multiport Measurements and Signal Leakage Problems

As noted above, even the first error models of a VNA included special error term(s) to address the influence of one system measurement port on another (i.e. the so-called leakage term, E_X). The leakage term was simply defined as a transmission coefficient between VNA ports being perfectly matched. This definition holds only for those cases when the DUT has input and output impedances equal to the system impedance. When measuring other devices, the application of a leakage term defined in such a way degrades the measurement accuracy.

Further measurement experiments and practical experiences revealed that the leakage can have a very complicated nature. It is generally insufficient to use just one or two error terms to correctly represent this phenomenon. Clearly, another description of systematic measurement errors was required.

Such a concept was introduced by Speciale and Franzen in 1977 [31]. The systematic measurement errors of the n-port VNA were represented by a $2n$-port virtual error network, connected with its n-ports to the DUT and its other n-ports to the ideal, error-free VNA. The error network consists of $(2n)^2$ coefficients and describes all possible influences of the measurement ports on each other. In fact, one error term can be set to be a free parameter and the error model can be normalized with respect to this term. That is, only $4n^2 - 1$ coefficients are linearly independent from each other. Thus, these error terms completely describe such a system [32].

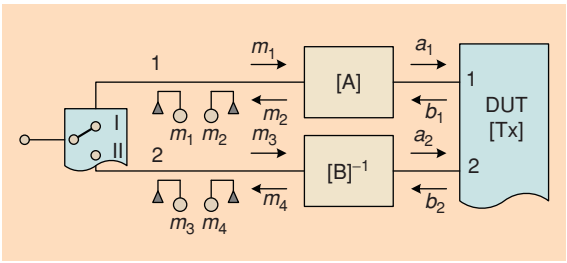


Figure 11. *Block diagram of VNA based on the double-reflectometer architecture. It shows the reference receivers,* m_1, m_3*; the signal source switch; the measurement receivers,* m_2 *and* m_4*; and the seven-term error model matrices* [A] *and* [B].

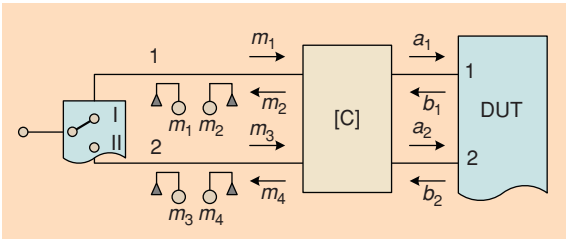


Figure 12. *Block diagram of the leaky VNA based on the double-reflectometer architecture. For the two-port system, the matrix* [C] *includes 15 error coefficients.*

The $4n^2 - 1$ model is only valid for VNAs built upon the double-reflectometer concept (with $2n$ measurement receivers, Figure 12). However, it was demonstrated much later that the full error model of a reference channel VNA (with $n + 1$ reference receivers) can also be defined (Figure 13). This includes significantly more error terms: e.g., 22 coefficients for a two-port VNA, compared with 15 coefficients for a two-port double-reflectometer VNA [33].

The error models including crosstalk describe the measurement system in a more general way. They can be easily transformed to their equivalent, crosstalk-free models by setting the crosstalk error coefficients to zero. Thus, the reduction of the 22-term model (for an $n + 1$ measurement receiver VNA) leads to a $(2n^2 + n)$-term crosstalk-free model (i.e., a ten-term model for the two-port case). Omitting the influence of the crosstalk from the $2n$ measurement receiver VNA ($4n^2 - 1$-term model) gives the $(4n - 1)$-term model (i.e., a seven-term model for the two-port case).

Partly Leaky Model

For some applications, the signal leakage between different measurement ports of a multiport system is not the same. For example, the multiport wafer-level measurement system configured with dual wafer probes (two ports per probe) shows a strong crosstalk between in-side (in-probe) ports, whereas the side-by-side (probe-to-probe) port influence is much lower. For such cases, it is feasible to include only those crosstalk coefficients in the system error model that most affect the measurement results.

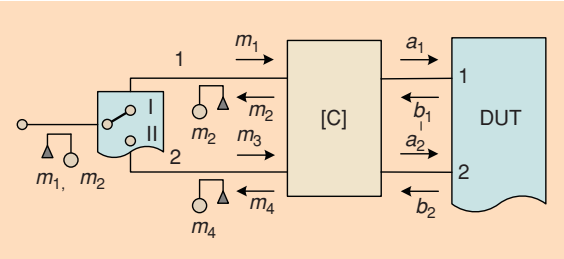


Figure 13. *Block diagram of the leaky VNA based on the reference channel architecture. For the two-port system, the matrix* [C] *includes 22 error coefficients.*

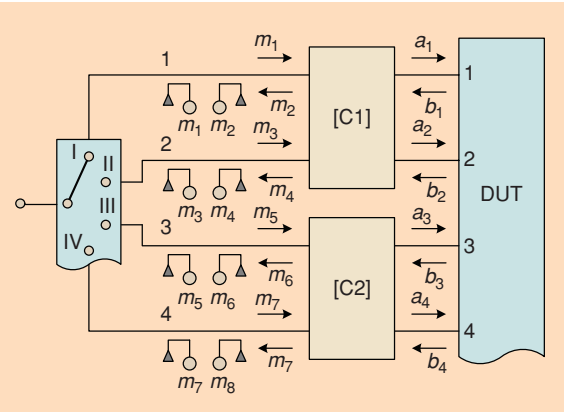


Figure 14. *A model of the double-reflectometer VNA allowing leakage between Ports 1 and 2 and between Ports 3 and 4.*

The solution for the four-port measurement system was introduced in [34]. In this case, the error network is split into two parts. Each covers the in-side ports only (e.g., one network [C1] for Ports 1 and 2 and a separate network [C2] for Ports 3 and 4, as shown in Figure 14). This approach significantly simplifies the description of the measurement system by reducing the number of error terms from $4n^2 - 1$ to $2n^2 - 1$, where n is the number of VNA ports. Thus, only 31 error coefficients (for the partly leaky model) are needed, instead of 63 error coefficients (for the fully leaky model), when describing a four-port VNA.

Once the error model is known, the error terms can be calculated with the help of the calibration procedure. Various calibration methods have been developed over the 40-year history of vector network analysis. Some of these methods became standard de facto methods, while others were just intermediate steps towards improving the accuracy of S-parameter measurements.

Calibration Procedures

First Iteration Solutions

Calibrating early VNAs was a lengthy and tedious process. Straightforward calculations of the required error terms as well as the error correction of the measured S-parameters of a DUT were not readily available at that time. Engineers were forced to rely on numerous variations of numerical and iterative procedures, e.g., [8].

First Explicit Solution

A significant advance was made in 1971 by Kruppa and Sodomsky [35]. For the first time, an explicit solution for calibrating a two-port VNA described by the eight-term model was introduced. This solution used three reflection standards (open, short, and match load termination) at each VNA port and two ports connected together (thru standard). Using the measurements of the open, short, and load at individual VNA ports, the three error terms S_{11}, S_{22}, and $S_{21}S_{12}$ (E_D, E_S and E_R) were defined for each port. The T_{21} and T_{12} terms were calculated from the forward and reverse transmission measurements of the thru standard, respectively (as shown in Figure 5).

The same work also introduced simple equations to perform a straightforward correction of the DUT's four S-parameters for the systematic measurement errors. Therefore, the need for lengthy iterative numerical calculations of error terms and error-corrected S-parameters was resolved.

This explicit approach was further modified for different test sets (error models) [20], [21] and, finally, the ten-term explicit calibration solution was introduced commercially by Hewlett-Packard in 1978 [19]. Since that time, this calibration procedure has become very popular under the name short-open-load-thru (SOLT) or thru-open-short-match (TOSM). Today, the SOLT calibration is a well-established technique that is implemented on all modern VNAs.

The accuracy of the SOLT procedure depends critically on the fabrication and modeling tolerances of the calibration standards (i.e., the lumped open, short, and load elements). Since the accuracy of these standards degrades with frequency, it remained a challenge to achieve reliable measurement results at high frequencies. Additional procedures, such as improving the calibration standard models (i.e., [36], [37]) or the use of standards initially characterized with respect to the reference calibration [38], can enhance the accuracy of the SOLT method.

Self-Calibration—TRL

The introduction of the TRL calibration (another variant of this is LRL) procedure by Engen and Hoer in 1974 was the next significant step in the development of VNA calibration theory [12]. For the first time, there was a method not requiring all standards to be either ideal or fully known. Using the redundancy of measurement results (an advantage of the double-reflectometer VNA and seven-term error model), TRL was able to define the originally unknown parameters of calibration standards like the reflection coefficient of the reflection standard and the propagation constant of the line standard. This new principle of calibrating a VNA with partly known standards was later called *self-calibration*.

Another advantage of the TRL technique is that it becomes possible to achieve real calibration and measurement traceability using well-defined air-isolated line standards. However, TRL is frequency limited. This restriction can be overcome by including additional line standards and applying a statistical analysis of the redundant measurement information (similar statistical techniques, such as weighted least squares [39] and generalized distance registration [40], have also been applied to one-port VNA calibration schemes resulting in a significant improvement in the overall accuracy of measurement), making TRL the accuracy benchmark per se [41]–[43].

TABLE 1. General requirements for the calibration standards.

Standard	Requirements
N1	Four known parameters (fully known)
N2	Minimum two known parameters
N3	Minimum one known parameter

Self-Calibration—Further Developments

After the introduction of the TRL self-calibration methods, many other different self-calibration procedures were developed. The measurement information redundancy obtained from the double-reflectometer VNA and its seven-term error model gives some calibration freedom: one or more standards may be partly unknown. This useful feature helps to define new calibration methods and optimize them for different applications.

For instance, the calculation of matrices $[A]$ and $[B]$ in Figure 9 can be performed by measuring three different two-port standards N_1, N_2, and N_3 instead of the DUT $[T]$ in (7)

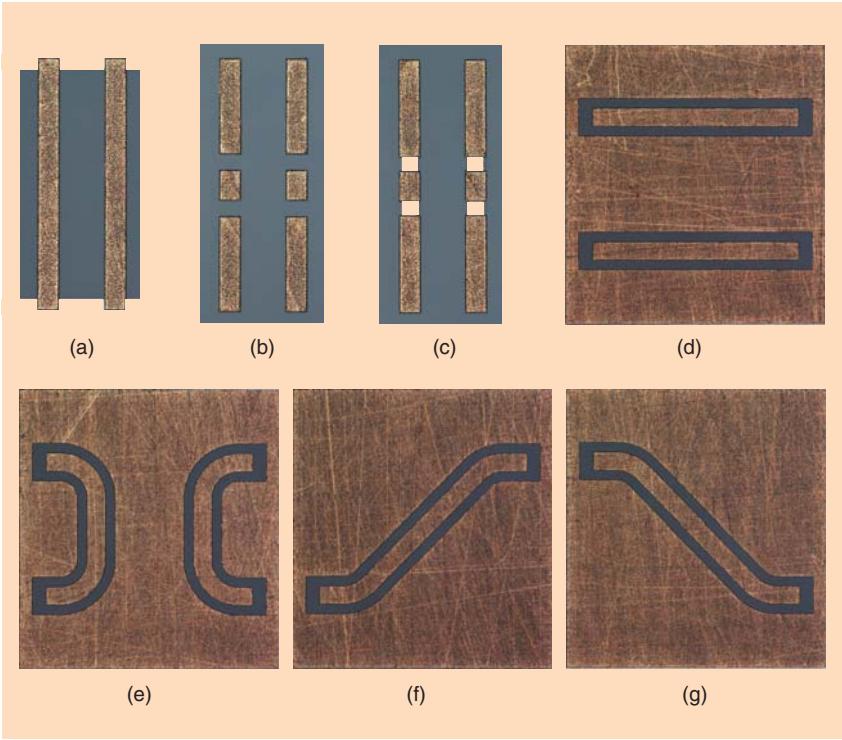


Figure 15. *Example of the commercially available (CSR) coplanar calibration standards: (a) paired shorts, (b) paired opens, (c) paired loads, (d) dual in-line thru lines, (e) dual loop-back thru lines, and, (f)–(g) cross-over thru lines. Such standards are used for most popular wafer-level calibration procedures.*

$$M_i = AN_iB^{-1}, (i = 1 \ldots 3). \quad (10)$$

To characterize the system completely [as in (6)], only seven unknowns have to be found from the 12 equations in (9). This redundancy produces general requirements to the calibration standards (Table 1) and makes it possible to derive many different calibration procedures [25], [44]–[46].

Reflection and transmission standards are addressed by the self-calibration procedure in two ways:

- one measurement of one known parameter (e.g., the reflection coefficient of a standard defines one error term)
- two measurements of the one unknown parameter taken under different conditions (e.g., the reflection coefficient of the same one-port standard measured at two VNA ports) give one error term.

Self-calibration requires seven error terms to be defined. In general cases, this can be met by any arbitrary combination of known and partly known standards (Figure 15). Today, TRL, line-reflect-match (LRM) [also often called thru-reflect-match (TRM) or thru-match-reflect (TMR)], short-open-load-reciprocal two-port (SOLR), quick-short-open-load-thru (QSOLT), and line-reflect-reflect-match (LRRM) are the most popular self-calibration procedures covering a very wide variety of applications.

Conventional and Improved LRM Procedures

The LRM method [47] was developed to resolve the frequency bandwidth limitation of conventional TRL. Instead of the line standard (or a set of different lines), it employed two one-port match (load) elements. Theoretically, LRM can be considered as a broadband calibration procedure. However, good calibration accuracy of commercially available LRM can be guaranteed only if using purely resistive, highly symmetrical 50Ω loads. This requirement is very difficult to achieve, especially at the wafer level. Some further improvements—like LRM, available from NIST [48], and line-reflect-match, advanced (LRM+) [49]—addressed this main drawback of conventional LRM.

SOLR

The SOLR method does not require the complete knowledge of the thru standard [50]. In fact, any passive two-port element providing a symmetrical (forward/reverse) transmission coefficient (reciprocal) can be used for the calibration. SOLR is very helpful for setups where implementation of the thru is impractical: e.g., for coaxial applications when measurement ports have the same sex, or rectangular port configurations at the wafer-level. The accuracy of the SOLR method strongly depends on the one-port standards (open, short, load), which have to be either ideal or fully known.

QSOLT

Like SOLT, the QSOLT procedure expects all standards to be fully known. However, it removes the need to measure the one-port standards at the second VNA port [51], [52]. This feature dramatically reduces the time spent on reconnecting and remeasuring the standards. However, it should be noted that a VNA calibrated with the QSOLT method exhibits significant measurement errors at its second port, i.e., the port that did not have the one-port standards connected to it during calibration [53].

LRRM

The LRRM procedure was the first method that was developed explicitly to address the needs of wafer-level applications. It was designed to resolve the restrictions of the planar lumped load, such as potential asymmetry and the frequency dependence of its impedance [54]. However, like QSOLT, it measures the load standards at only one VNA port. For some applications, this may lead to less reliable measurement results at the second VNA port [55].

Table 2 gives a brief comparison of these popular self-calibration procedures for the following criteria:

- type of calibration standards
- use of standards
- definition of error term (ET) from reflection and transmission measurements
- products obtained from the redundancy information.

Calibration of the Leaky System

Obviously, calibrating a leaky system (e.g., described by the 15-term models) requires an extended number of standards and/or calibration measurements. An iterative solution for the 15-term model was presented in [56]. It proposed four fully known two-port standards: one standard was the thru, while the remaining three standards were combinations of match-match, open-short, and short-open elements. As shown later in [57], the use of only four fully known two-port standards leads to an undetermined system of equations and, ultimately, a reduction in calibration accuracy. At least five such standards are required.

The explicit calibration and some self-calibration solutions for the 15-term model have been presented [57]–[60]. Also, the work in [33] gave a solution for the reference channel system (i.e., the 22-term model). Finally, the general self-calibration match-unknown-reflect-network (MURN) method for a leaky system was presented with eight unknown parameters of standards [58].

Multiport Cases and Hybridization

The fact that both ten-term and seven-term system descriptions can be applied to the multiport reflectometer VNA gives the user enough flexibility in choosing the most appropriate calibration method for his or her measurement system applications. Since the seven-term calibration procedures are insensitive to inaccuracies in some standards, this often makes them the preferred choice (e.g., [61], [62]).

When calibrating the seven-term system, selected error terms can be calculated using different methods. For instance, one can perform a hybrid calibration with a combination of SOLR and LRM [63] or another method [64]. This approach has benefits when some thru standards are difficult to characterize (e.g., at wafer level). However, hybrid methods may have limitations concerning the calibration dynamic range because they are based on the seven-term model [65].

An alternative way of integrating the advantages of different calibration procedures has been proposed by [66] and [67] with the generalized reflect-reflect-match-thru, advanced (GRRMT+) multiport solution. In contrast to hybrid calibrations, the GRRMT+ procedure uses the seven-term-based self-calibration LRM+ and SOLR procedures to calculate the accurate behavior of the partly known standards (i.e., the reflects and the thrus). Once all calibration standards are fully known, error terms are

TABLE 2. Comparison of TRL, LRM, SOLR, QSOLT, and LRRM calibration procedures.

	TRL		LRM/LRM+		SOLR		QSOLT		LRRM	
	Port 1	**Port 2**	**Port 1**	**Port 2**	**Port 1**	**Port 2**	**Port 1**	**Port 2**	**Port 1**	**Port 2**
Transmission Standards										
THRU Four Known S-parameters	☑ (4 ET)		☑ (4 ET)		×		☑ (4 ET)		☑ (4 ET)	
LINE Known: S_{11}, S_{22} Unknown: S_{21}, S_{12}	☑ (2 ET)		×		×		×		×	
RECIPROCAL Known: $S_{21} = S_{12}$, Known for $+/-90$ Degree Unknown: S_{11}, S_{22}	×		×		☑ (1ET)		×		×	
Sum of Error Terms Defined from Transmission Measurements	6		4		1		4		4	
Reflection Standards										
	Port 1	**Port 2**	**Port 1**	**Port 2**	**Port 1**	**Port 2**	**Port 1**	**Port 2**	**Port 1**	**Port 2**
OPEN One Known Per Port	×	×	×	×	☑ (1 ET)	☑ (1 ET)	☑ (1 ET)	×	×	×
SHORT One Known Per Port	×	×	×	×	☑ (1 ET)	☑ (1 ET)	☑ (1 ET)	×	×	×
LOAD One Known Per Port	×	×	☑ (1 ET)	☑ (1 ET)	☑ (1 ET)	☑ (1 ET)	☑ (1 ET)	×	☑ (1 ET)	×
REFLECT $S_{11} = S_{22}$, Known for $+/-90$ Degree One Known for Two Ports	☑ (1 ET)		☑ (1 ET)		×		×		☑ (as open) (1 ET) ☑ (as short) (1 ET)	
Sum of Error Terms Defined From Reflection Measurements	1		3		6		3		3	
Self-Calibration Product	Reflection Coefficient of the Reflect Propagation Constant of the Line		Reflection Coefficient of the Reflect		S-Parameters of the Reciprocal		No		Reflection Coefficient of both Reflects	

calculated by the modified GSOLT procedure with nonideal, but known, standards. Thus, the limitations of the multiport ten-term, multiport seven-term, and hybrid methods are overcome all in one procedure.

Future Perspectives

In the last four decades, we have observed remarkable advances in microwave measurement instrumentation as well as in calibration and error correction methodologies. This significantly influenced the evolution of high-frequency semiconductor devices. Precise measurement results are crucial for understanding the real performance of a DUT, verifying its model, and improving its design. Thus, progress in the *S*-parameter measurement methods accelerated the development of, for example, high-performance telecommunication and defense systems.

Today's progress in wireless technologies and high-frequency broadband applications and the requirements for low power consumption, reduced electro-magnetic interferences, increased sensitivity, and increased data transfer rates drive the development of high-frequency passive and active differential devices. Therefore, the improvement of measurement systems is integral for providing broadband differential driving signals.

The first multiport VNAs enabling true differential measurement are already commercially available [68], [69]. Some methods for correcting systematic measurement errors have recently been published [70], [71]. These methods represent modifications of existing approaches for single-ended systems. The next significant step in calibration and error correction theory could well be the introduction of true-differential error models and calibration standards. New straightforward true-differential calibration methods will drastically simplify the calibration process. It will bring the accuracy of measurement and characterization of differential devices to new levels.

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13 ATTACHMENT TO CHAPTER 3

13.1 Paper [50]: “Verification of the wafer-level LRM+ calibration technique for GaAs applications up to 110 GHz”

R. Doerner and A. Rumiantsev, "Verification of the wafer-level LRM+ calibration technique for GaAs applications up to 110 GHz," in *ARFTG Microwave Measurements Conference-Spring, 65th*, 2005, pp. 15-19.

In this article the accuracy of the transfer TMR calibration was compared to that of the benchmark NIST multiline TRL procedure for the first time. The comparison was performed on NIST verified GaAs coplanar waveguide calibration reference material RM8130. The NIST calibration comparison method was used to quantify the difference between measured S-parameters corrected by NIST multiline TRL and the transfer TMR. The worst-case error bounds for TMR corrected S-parameter measurements were determined up to 110 GHz. It was demonstrated that the difference between the benchmark multiline TRL and transfer TMR was comparable with the measurement system drift.

In this paper, I developed the verification methodology, planned the work and wrote the main part of the paper. My coauthor Ralf Doerner from Ferdinand-Braun-Institut (FBH), Leibniz-Institut fuer Hoechstfrequenztechnik (Berlin, Germany) made all required measurements. We shared calculation and the data analysis.

Verification of the Wafer-Level LRM+ Calibration Technique for GaAs Applications up to 110 GHz

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***Abstract* — In this article the accuracy of the LRM+ calibration is compared to that of the benchmark NIST multiline TRL procedure for the first time. The comparison is performed on NIST verified GaAs coplanar waveguide calibration reference material 8130. The NIST calibration comparison method is used to quantify the difference between measured S-parameters corrected by NIST multiline TRL and an advanced LRM+ calibration. The worst-case error bounds for LRM+ corrected S-parameter measurements are determined up to 110 GHz. It is demonstrated that the difference between benchmark multiline TRL and LRM+ is comparable with the measurement system drift. Verification results prove that LRM+ can be successfully used for accurate GaAs on-wafer calibration with customized standards. This overcomes some drawbacks of multiline TRL while providing the same calibration accuracy.**

***Index Terms* — calibration, error correction, calibration comparison, scattering parameters measurement.**

I. Introduction

First attempts to calibrate wafer-level RF measurement set-ups were performed in the beginning of the 1980's. Yet, the verification of wafer-level calibration accuracy has remained a critical issue. Different calibration procedures have been developed in the past years (i.e. [1]–[7]). All of them rely on ideal, fully or partly known reference elements (calibration standards), realized in planar design (microstrip or coplanar).

In contrast to coaxial and waveguide applications, a great variety of fabrication techniques makes it almost impossible to trace back planar calibration standards to a natural reference. This substantially complicates the task of specifying and verifying planar calibrations.

However, research undertaken by the National Institute of Standards and Technology (NIST) provided a procedure comparing wafer-level calibrations to those performed by NIST [8]. It can be used by industrial laboratories for verification purposes. With the help of this approach, the LRM+ [7] procedure has been compared to a well-defined benchmarking multiline TRL calibration developed by NIST [2].

As demonstrated in [7], accurate measurement results can be achieved up to 110 GHz on conductive wafers using LRM+ and a customized set of standards. However, although results presented in [7] verify the calibration accuracy qualitatively, the quantitative verification of the LRM+ procedure is still a challenge.

Several accuracy verification procedures for on-wafer calibration are currently in use, e.g. [9], [10]. But almost all of them rely on error-corrected measurements of well-known reference elements. The difficulty to realize an ideal verification element on the test wafer reduces the accuracy of such approaches.

In contrast to this, a method to define error boundaries of error-corrected measurements, in relation to a well-defined calibration, was proposed in [8] and realized in a software package developed by NIST.

This method is used here in order to assess accuracy of the LRM+ procedure quantitatively. The following section briefly describes the verification approach used while Section III presents experimental results.

II. Verification Procedure

A. Calibration Comparison Procedure

The procedure used for accuracy verification provides the worst-case deviations of the measured S-parameters of passive devices for the examined (first-tier) calibration with respect to the benchmark (second-tier) calibration. Deviations are treated as $|S_{ij}-S_{ij}'|$, for $ij \in \{11, 12, 21, 22\}$, where S_{ij}' is the S-parameter measured by the calibration to be tested, and S_{ij} is the S-parameter measured by the benchmark calibration.

NIST multiline TRL was selected as the benchmark calibration. In conjunction with methods proposed in [12] and [13], this procedure allows accurate setting of the measurement system reference impedance to 50 Ohm as well as a precise definition of the measurement reference plane.

Both the LRM+ and the benchmark multiline TRL calibration were performed on the semi-insulating GaAs reference material 8130 (RM 8130), provided by NIST.

B. Reference Material 8130

The RM 8130 consists of a coplanar wave guide (CPW) multiline TRL calibration set: a 550 μm long thru line, five lines with lengths of 2.685 mm, 3.75 mm, 7.115 mm, 20.245 mm, and 40.55 mm, and two offset shorts located in a distance of 225 μm from the beginning of the line. There are

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also additional 12 verification reference elements. For the LRM+ calibration we use the 550 μm thru line, the 225 μm offset short, and two offset loads. The paired load standard with the resistance of about 73 Ohm for both ports was used for the first LRM+ calibration, while the asymmetrical verification resistor with the port 1 resistance of about 46 Ohm and port 2 resistance of about 133 Ohm was used for the second LRM+ calibration.

According to the individual test results provided by NIST for every RM 8130, the actual line capacitance is 1.7877 pF/cm. This value is used by the benchmark multiline TRL calibration for the accurate definition of the characteristic impedance of the RM 8130 lines and the transformation of the measurement system reference impedance.

C. Wafer-Level Measurement Setup and Software

The experimental setup for the 110 GHz wafer-level measurements includes an Agilent 8510XF VNA, a manual wafer-probe station, and the 110 GHz wafer probe tips having a pitch of 125 μm. The examined first-tier LRM+ calibration was performed using external calibration software[1]. The second-tier benchmark multiline TRL calibration as well as the accuracy analysis was performed with the help of the MultiCal® software package[2].

III. Experimental Results

To avoid additional contact uncertainty, all RM 8130 calibration standards required for benchmarking multiline TRL and the LRM+ as well as the reference elements were measured in one measurement series in the frequency range from 150 MHz up to 110 GHz. At the end of the experiment, the multiline TRL calibration standards were re-measured providing the second measurement series.

A. Verification of the Measurement Setup Integrity

First, stability of the measurement instrument and its capability to reproduce NIST measurements was validated using a multiline TRL calibration, GaAs reference material RM 8130, and the software package MultiCal©. Acquired data were corrected externally, using the multiline TRL procedure and compared to the reference data provided with the RM 8130 by NIST. The second measurement series of TRL calibration standards was used to define the drift of the measurement setup within the experiment. Obtained results are presented in Fig. 1. They are limited to 40 GHz due to the frequency limitation of the original RM 8130 measurement reference data.

According to [11], this bound increases with frequency and should not exceed 0.1 up to 40 GHz. As demonstrated in Fig. 1, the measurement setup generally meets this requirement. Thus, it forms a reliable basis for calibration comparison purposes. However, some discontinuities detected around 35 GHz may deteriorate verification accuracy in the range 32…39 GHz. Also, it has to be noted that due to the hardware limitation of the VNA it was not possible to measure accurately below 500 MHz. So, measured and calculated data below 500 MHz were not taken into consideration.

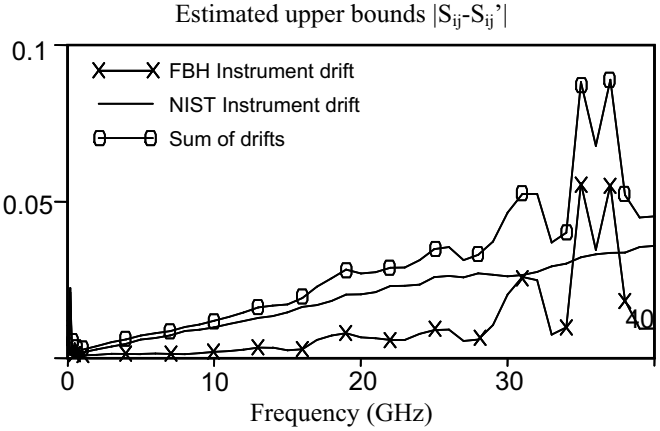

Fig. 1. Verification results on integrity of the wafer-level measurement setup used.

B. Accuracy and Repeatability Verification of the LRM+

In a second step, a multiline TRL calibration up to 110 GHz was performed for data obtained from the first and the second measurement series. The measurement system reference impedance was set to 50 Ohm and the measurement reference plane was defined at the center of the RM 8130 550 μm thru standard. The measurement system drift was determined up to 110 GHz from the second measurement series of all required multiline TRL standards by a second-tier multiline TRL.

Electrical parameters of a paired load standard (Load 1) were calculated for both cases. As shown in Fig. 3, the loads are almost symmetrical and have a resistance different from 50 Ohm (approximately 73 Ohm) and an additional reactive part. Loads are slightly dispersive. As discussed in [7], standards of this kind can be successfully used for the LRM+ calibration.

In the next step, two LRM+ calibrations were performed up to 110 GHz using the first and the second measurement series. The system reference impedance was set back to 50 Ohm by means of an LRM+ algorithm for each port individually. According to the calibration comparison technique proposed

[1] The LRM+ calibration procedure is implemented in the commercially obtainable software SussCal® from SUSS MicroTec.

[2] The MultiCal® package is provided by National Institute of Standards and Technology.

in [11], a second-tier multiline TRL calibration was used as benchmark calibration to determine the upper error bound for both cases.

The error bounds of these two LRM+ calibrations as well as a measurement system drift are shown in Fig. 2. It is obvious that the difference between the first and the second LRM+ calibration is marginal. Experimental results prove that both LRM+ calibrations provide the same measurement accuracy as the benchmarking NIST multiline TRL up to 110 GHz. The variation of the measurement accuracy is comparable with the measurement system drift over the whole frequency range.

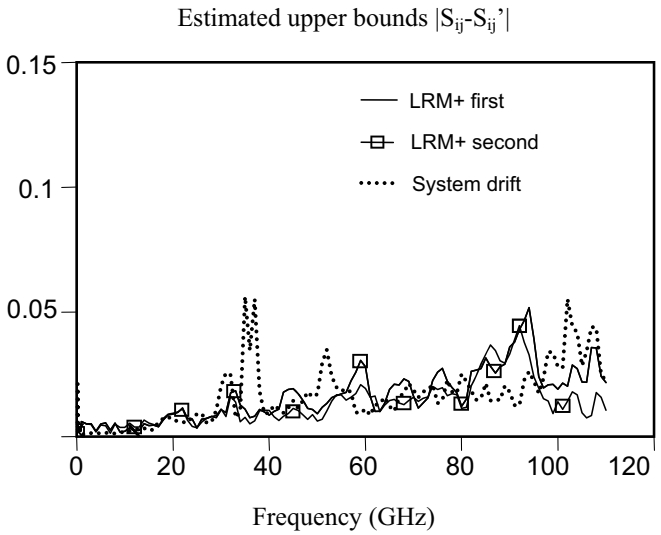

Fig. 2. The maximum possible differences from the benchmark NIST multiline TRL calibration for two 110 GHz LRM+ calibrations and actual system drift.

C. LRM+ with Asymmetrical Load Standard

A combination of two different load elements was used for the next experiment, namely the port-1 element of the RM 8130 verification resistor (see Fig. 3, Fig, 4, Load 2: Z11) and the port-2 element of the RM 8130 load standard used in the previous experiment (see Fig. 3, Fig. 4, Load 1: Z22). This combination artificially repeats the calibration conditions typically occurring in practice for customized wafer-embedded LRM calibration kits. The load model was defined based on measurement data corrected with the multiline TRL.

Using this load combination together with the 550 μm thru and the offset short, four different variants of the LRM calibration procedures can be performed: the simple LRM [3], the LRM, normalized to the port-2 load impedance [4], the LRM+ with the DC load (R1 = 45.92 Ohm, R2 = 72.71 Ohm) correction, and the LRM+ with the complete correction of the load standard imperfectness. The accuracy of each of them was compared to the benchmark multiline TRL. Fig. 5 presents the experimental results.

As expected, the simple LRM differs from the benchmarking multiline TRL by a value of about 0.6 over the whole frequency range. The estimated measurement error of a simple LRM procedure in the low-frequency range is caused by the deviation of the load resistance from 50 Ohm and its port asymmetry. Fig. 3 shows that the real part of the port-1 impedance is nearly constant over frequency. At the same time, the imaginary part increases slightly (Fig. 4). The real part of the port-2 load impedance decreases with frequency, while its imaginary part increases. This results in a nearly constant port asymmetry of the load standard used.

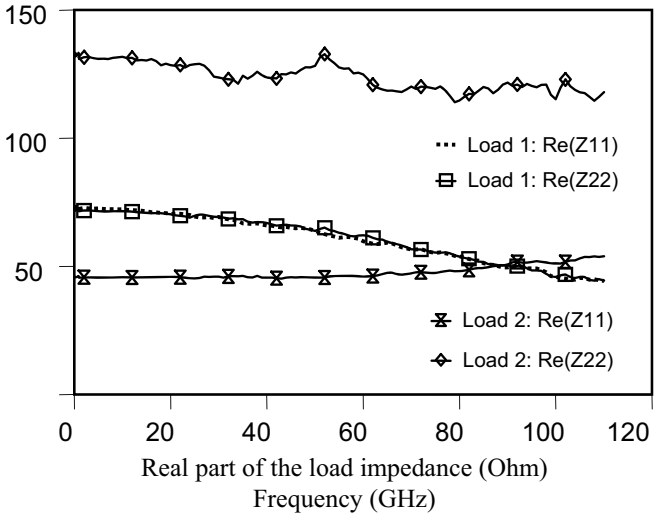

Fig. 3. The real part of the measured port 1 (Z11) and port 2 (Z22) impedance of the load standard (Load 1) and a resistor (Load 2), located on the RM 8130.

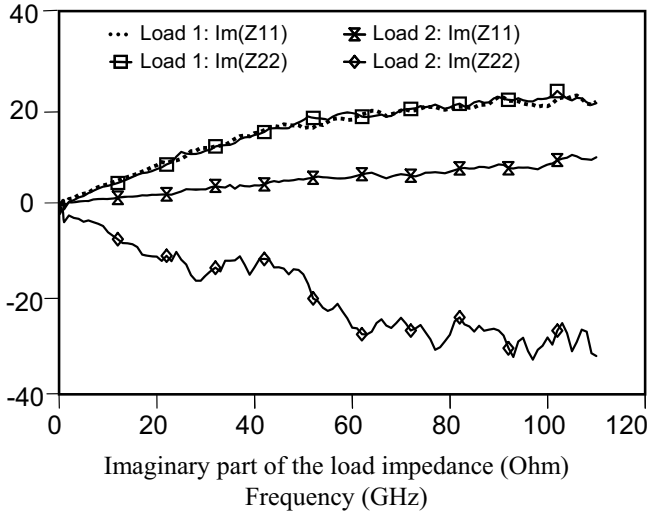

Fig. 4. The imaginary part of the measured port 1 (Z11) and port 2 (Z22) impedance of the load standard (Load 1) and a resistor (Load 2), located on the RM 8130.

Normalizing LRM to the impedance of the port-2 load provides better accuracy beyond 40 GHz than using the simple LRM. This arises from the decreasing difference in magnitude of the load impedances at both ports due to their reactive parts.

Results for the DC load corrected LRM+ generally correspond to those presented in [4]. However, in contrast to the experimental results, the procedure from [4] used the same load standard for both calibration ports.

The complete LRM+ calibration provides the best accuracy with full individual correction of the load imperfectness for each measurement port. The upper error bounds are comparable with the system drift. It has to be noted that the LRM+ error bounds of this experiment are comparable with those found in Section III.B (Fig. 2), while the used load standard was strongly asymmetrical.

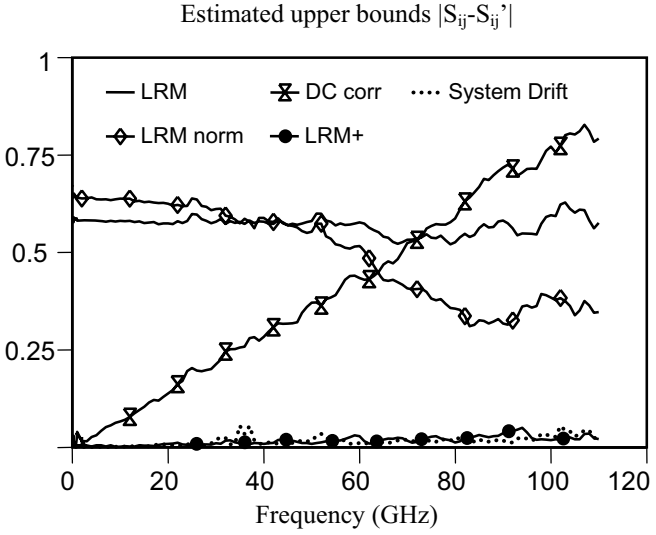

Fig. 5. The maximum possible differences between measurements of passive devices from NIST multiline TRL calibration for the simple LRM, the normalized LRM, the DC load corrected LRM+, and the complete LRM+ calibration.

D. Port Symmetry Verification

Accurate calibration aims for the exact definition of the reference impedance at both ports to the same value (i.e. 50 Ohm). As discussed in [5], LRM-like procedures set the reference impedance to the impedance of the load standard. Typically, on-wafer load standards are realized in pair. This should provide measurements of identical loads at both ports. Supposed that these loads are not equal (i.e. due to the fabrication tolerances), the reference impedance will involve errors, with regard to both the desired value and the difference between ports. The observed effect is called "port asymmetry": measurements of the same one-port device show different results at each port. The positive or negative offset from the expected value depends on the amount of the load asymmetry. To avoid this, either the load standard has to be realized symmetrically or its asymmetry should be accounted for by the calibration procedure.

The series attenuator embedded in RM 8130, symmetrical for return loss measurements, was used to verify the port symmetry of simple LRM, normalized LRM, DC load corrected LRM+, and the complete LRM+. The verification results are presented in Fig. 6. In contrast to other LRM procedures, the return loss measurements of the attenuator corrected by LRM+ calibration are highly symmetrical. The results of port symmetry verification obviously correspond with those obtained from the calibration verification (Fig. 5). Again, it is demonstrated clearly that conventional LRM-like procedures do not yield sufficient calibration accuracy for non-symmetrical non-ideal load standards.

The method [8], which is used in this work for the accuracy analysis of different LRM calibrations, also covers the measurement error caused by the "port asymmetry" problem. However, there are cases where this method is not applicable (i.e. for conductive wafers, or if the RM 8130 is not available). As demonstrated, the measurement of a suited symmetrical two-port element provides an alternative tool to verify calibration accuracy utilizing the port symmetry.

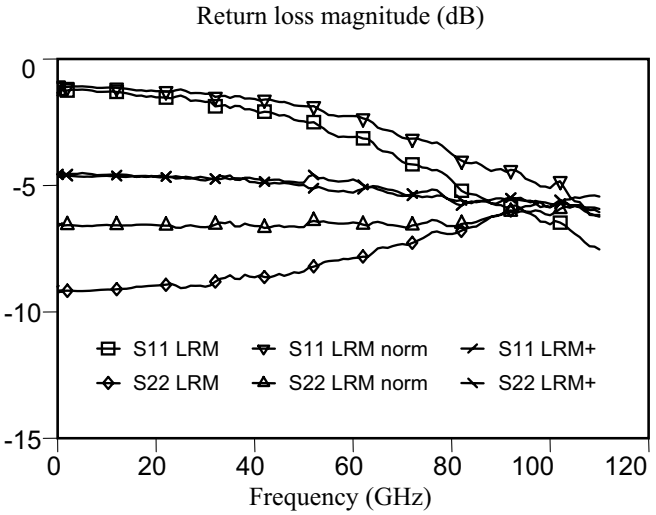

Fig. 6. Results of port symmetry verification for the LRM, the normalized LRM, and the LRM+ calibration using the RM 8130 series attenuator.

IV. Conclusions

Summarizing one can state that our experimental results demonstrate that the difference of benchmarking multiline TRL and LRM+ accuracy is comparable to the measurement system drift over the whole frequency range studied (500 MHz…110 GHz). This proves LRM+ to be a valuable tool as it overcomes the main drawback of multiline TRL: LRM+ does not require a large set of calibration standards but

nevertheless provides calibration accuracy comparable to the NIST multiline TRL. LRM+, therefore, saves wafer space, minimizing the test chip size to only three standards, realized in the same design. Thus, a fully automated calibration is possible even when using a fixed wafer probes configuration. The required determination of the electrical model of the used load standards can be done easily, e.g., by means of the approaches presented in [7], [14]. As shown above, LRM+ can be successfully used for GaAs applications up to 110 GHz.

ACKNOWLEDGEMENT

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13.2 Paper [52]: “Advanced on-wafer multiport calibration methods for mono- and mixed-mode device characterization”

H. Heuermann, A. Rumiantsev, and S. Schott, "Advanced on-wafer multiport calibration methods for mono- and mixed-mode device characterization," in *ARFTG Microwave Measurements Conference-Spring, 63rd,* 2004, pp. 91-96.

This paper outlined the theoretical background and the results of advanced RF calibration procedures especially suited to support wafer level RF device characterization with mono and/or mixed-mode interfaces. Based on the large number of possible methods to combine two-port calibration algorithms with multiport techniques, two methods were derived and investigated focusing on on-wafer devices. The results of our experiments demonstrated the effectiveness of the novel RRMT on-wafer calibration method for multiport devices.

In this work, I was responsible for collecting measurement data and data analysis. My co-author Prof. Holger Heuermann (Fachhochschule Aachen, Germany) developed the mathematical solution. Steffen Schott (SUSS MicroTec, Germany) organized the access to a 4-port VNA.

Advanced On-Wafer Multiport Calibration Methods for Mono- and Mixed-Mode Device Characterization

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***Abstract*— This paper outlines the theoretical background and the results of advanced RF calibration procedures specially suited to support wafer level RF device characterization with mono- and/or mixed-mode interfaces. The analysis of on-wafer measurement systems bring up the benefits of using load standards, reflectometers, as well as the GSOLT-model to perform high quality device characterizations. Based on the large number of possible methods to combine two-port calibration algorithms with multiport techniques, two methods were derived and investigated focusing on on-wafer devices. The results of our experiments demonstrate the effectiveness of novel RRMT on-wafer calibration method for multiport devices.** [1]

I. Introduction

The accurate modeling of microwave devices is necessary to develop communication products on low cost semiconductors and MMICs. A correct modeling of semiconductors needs precise on-wafer measurement data. To ensure the validity of the measured data, the RF test equipment must be calibrated.

In the past decades, many RF calibration methods for two-port scattering parameter measurements have been published and many of them are established [1]–[6]. Meanwhile, for both network analyzer architectures, the reflectometer-concept and the reference-channel concept, multiport calibration methods are published [7], [8].

The purpose of the presented work was to design a multiport calibration procedure, which is optimized for on-wafer conditions. The algorithm must support mono- and mixed-mode interfaces, [9].

This paper describes the requirements of an on-wafer measurement system for multiport devices, including calibration standards, vector network analyzer (VNA) architectures as well as error-correction algorithms. A new and very short theory for calibration and error-correction of multiport VNAs based on the reflectometer-concept is presented. The results of sections IV and V introduce the multiport-LRRM[2]- and the novel RRMT[3]-procedures. Results representative of the RRMT-method show that this procedure is a very robust and accurate calibration method.

II. On-Wafer Measurement System

Users of VNAs for measurements of devices with coaxial standards are not familiar with on-wafer calibration and error-correction techniques. However, RF engineers, performing on-wafer measurements, are familiar with calibration methods and the necessary standards. The reasons being the complexity of on-wafer standards and the on-wafer devices under test (DUTs) which are critical components for accurate modeling of the devices. Therefore, calibration methods are established for one- and two-port on-wafer measurements. The most often used methods are SOLT[4], [19], and the self-calibration procedures TRL[5], [1], LRM[6], [3], and LRRM (Line/Reflect/Reflect/Match), [4], [12].

SOLT relies on fully known standards, which is difficult to achieve at wafer level beyond 40 GHz, [13], [14]. In contrast to the SOLT, the advantage of the self-calibration procedures (e.g. TRL, LRM, etc.) is that the reflection standard uncertainty (radiation, losses, and an imperfect phase behavior) can be ignored without any affect to the calibration accuracy.

The inability to compensate for imperfect transmission lines limits the on-wafer TRL frequency range [13]. Other TRL drawbacks include multiple transmission lines, repositioning the probes and the requirement of the very long transmission lines for low frequencies [20].

Conventional LRM calibration sets the reference impedance to the value of the ideal match standard. NIST LRM uses an arbitrary match, but the match must be similar for both ports [6]. LRRM [4], [12] like the QSOLT procedure, [17], relies on the measurements of the load standard at one port only. This approach is free of the possible port's asymmetry of the planar load standard, but it sets the reference impedance of the second measurement port inaccurately [18].

To perform a self-calibration without any systematic error, a VNA based on the reflectometer architecture is needed. This kind of VNA has, in the three-port case, six measurement channels as shown in Fig.1. The basics of a multiport calibration for this kind of VNA are based on the 7-term model and are published in [7].

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[2] LRRM is the abbreviation for Line/Reflect/Reflect/Match.

[3] RRMT is the abbreviation for Reflect/Reflect/Match/Thru.

[4] SOLT is the abbreviation for Short/Open/Line/Thru

[5] TRL is the abbreviation for Thru/Reflect/Line

[6] LRM is the abbreviation for Line/Reflect/Match

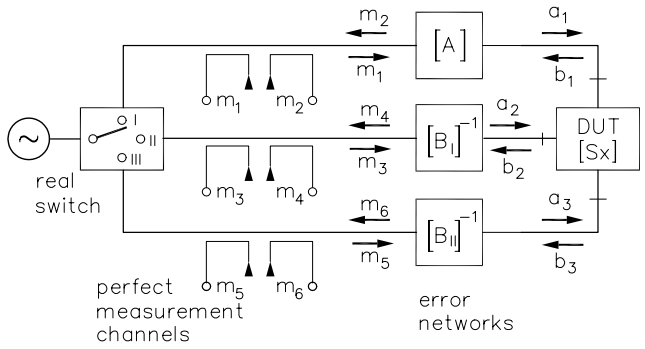

Fig. 1. Block diagram of a 3-port vector network analyzer with three ports and six measurement channels (triple-reflectometer)

However, for the VNA architecture with less measurement channels, (Fig. 2) a different multiport method was published, [8], which is based on the 10-term model[7]. This GSOLT[8] method can also be used for VNAs, based on the reference-channel or reflectometer concept.

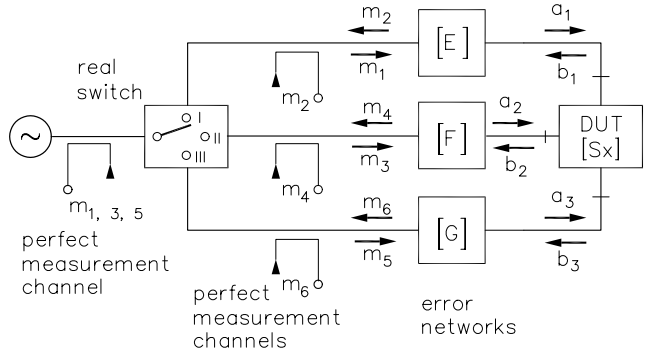

Fig. 2. Block diagram of a 3-port vector network analyzer with four measurement channels (reference-channel architecture)

In comparison between the two calibration procedures, the 7-term model and the 10-term model shows avowedly that the 7-term procedure has so-called bracings, [11]. The main dilemma of these bracings are, that the error-corrected measurements do not include the full transmission dynamic performance. Procedures using the 10-term model are much more robust.

Because of this deficiency, for multiport on-wafer calibrations we combined the GSOLT-technique and the LRM-procedure, which results in the RRMT-method. We compared RRMT with another multiport 7-term model calibration procedure, which also required two unknown reflection standards but only one match.

Next a simplified theory for the multiport 7-term model is presented.

[7]The 10-term model is the basic model of the 12-term SOLT-model.
[8]The name GSOLT is the short form of *General SOLT*.

III. Theory of GTXX

The way to calibrate or to error-correct the multiport VNA with the GTXX[9]-procedure is described by using a three-port triple reflectometer VNA. These results can easily be extrapolated to n-port VNAs. The block diagram with the error networks of a three-port triple-reflectometer VNA is shown in Fig. 1. The block diagram shown in Fig. 1 can be separated into two double-reflectometer VNAs: Using the first and second state of the switch, the error matrices $[\mathbf{A}]$ and $[\mathbf{B_I}]^{-1}$ can be calculated with a standard two-port calibration TXX-procedure, [5], as well as any method which fits the 7-term model, e.g. TRL. With the first and third state of the switch, the 7 parameters of the error boxes $\mathbf{A}$ and $\mathbf{B}_{II}$ can also be calculated by using a TXX-procedure.

The notation is using the transmission parameters

$$[\mathbf{Mx}] = [\mathbf{A}]\,[\mathbf{Nx}]\,[\mathbf{B_i}]^{-1} \tag{1}$$

with the measurement matrix $[\mathbf{Mx}]$ for the DUT $[\mathbf{Nx}]$, [5].

The number of error coefficients is 3 for the error box $\mathbf{A}$ and $4*(n\text{-}1)$[10] for the transmission calibration steps, i.e. $4*n\text{-}1$ error coefficients in total.

A. GTXX Error Correction Process

It is useful to invert the error matrices for the GTXX multiport error correction process.

$$[\mathbf{G}] = [\mathbf{A}]^{-1}\ , \quad [\mathbf{H_i}] = [\mathbf{B_i}]^{-1}\ , \quad (i = I, II) \tag{2}$$

Referring to Fig. 1, the relations

$$\begin{pmatrix} b_1 \\ a_1 \end{pmatrix} = [\mathbf{G}] \begin{pmatrix} m_1 \\ m_2 \end{pmatrix}\ , \tag{3}$$

$$\begin{pmatrix} b_2 \\ a_2 \end{pmatrix} = [\mathbf{H_I}] \begin{pmatrix} m_3 \\ m_4 \end{pmatrix}\ , \quad \begin{pmatrix} b_3 \\ a_3 \end{pmatrix} = [\mathbf{H_{II}}] \begin{pmatrix} m_5 \\ m_6 \end{pmatrix} \tag{4}$$

hold in every state of the switch for the inverted transmission parameters. That means that for a three-port, all three sets of error corrected incident and reflected wave values

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \end{pmatrix} \tag{5}$$

can be calculated with high accuracy.

Finally, we can combine the three sets of S-parameter equations to the matrix equation

$$\underbrace{\begin{pmatrix} b'_1 & b''_1 & b'''_1 \\ b'_2 & b''_2 & b'''_2 \\ b'_3 & b''_3 & b'''_3 \end{pmatrix}}_{=[\mathbf{K}]} = \underbrace{\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix}}_{=[\mathbf{Sx}]} \underbrace{\begin{pmatrix} a'_1 & a''_1 & a'''_1 \\ a'_2 & a''_2 & a'''_2 \\ a'_3 & a''_3 & a'''_3 \end{pmatrix}}_{=[\mathbf{L}]} \tag{6}$$

and use the equation

$$[\mathbf{Sx}] = [\mathbf{K}]\,[\mathbf{L}]^{-1} \quad . \tag{7}$$

to calculate the error-corrected S-parameters.

[9]GTXX stands for *General TXX*.
[10]n: Number of the measurement ports.

B. A Comparison of GSOLT and GTXX

The advantages of GTXX:

- Less calibration measurements.
- Many possible self-calibration standards.
- Easy to create calibration standards can be used.
- Switch can have poor isolation.

The advantages of GSOLT:

- Less measurement channels = cheaper VNAs.
- More robust for high dynamic measurements.

To overcome the drawback of GSOLT for on-wafer measurements which require perfect open and short standards, we have derived GSOLT in the most general way of three reflection standards with known but not ideal reflection parameters. Using this common approach we are able to use the results of TXX self-calibration algorithms, which were already done for RRMT.

IV. Theory of Multiport-LRRM-Procedure

The theory of the two-port LRRM method is well-known, [4], [12], by using the standards shown in Fig. 3.

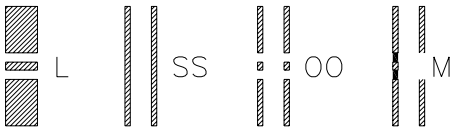

Fig. 3. Calibration standards of the LRRM-procedure

Since the match standard is only contacted at one port, the GSOLT-model can not be used for the multiport procedure. Thus we described in [10] how to realize the multiport-LRRM-procedure based on GTXX.

V. Theory of the Novel RRMT-Procedure

It is well known that the self-calibration process works with high accuracy for the reflection standards. In addition, only a thru and a load are attractive candidates for on-wafer measurements. The assumption that the loads are identical and the used 7-term model are the reasons for the so-called bracings of the conventional LRM procedure. The traditional solution to overcome this problem the measurement of the load standard at one port only (e.g. LRRM procedure). However, as described in [10] and [21], this approach has many other drawbacks.

Our new solution to overcome the bracing problem of conventional LRM is the RRMT-procedure. The RRMT procedure consists of the following steps: We use the self-calibration process to calculate the accurate values of the open and the short standard (The bracing of the LRM-procedure have only negligible effect on the calculation of the highly reflective self-calibration values). We use, for the calculation of the R-standards, the most robust formula for 7-term procedures, [5]. We already have four well-known standards: R1=S, R2=O, M=L, T, all with non-ideal but known values. So, we derive the GSOLT-procedure with non-ideal values. The mathematical derivation is the same as the presented GSOLT, [2], [8], but the equations are much more complex, [10].

In this way, RRMT uses the benefits of the LRM-technique and the robustness of the GSOLT-procedure (10-term model) respectively. Errors in the match standards have no influence on the measurement's performance apart from the fact that the real values of the match standards establish separate system impedances for the forward and the reverse direction scattering parameters. The last can be easily overcome defining the arbitrary match standard for each port independently according to [13], [15], [16], and [21].

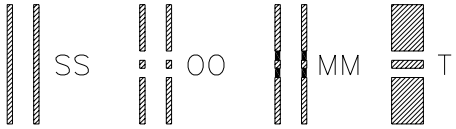

Fig. 4. Calibration standards of the RRMT-procedure

VI. Measurement Results

We used the multiport network analyzer from Ballmann[11] over the frequency range of 1 GHz to 6 GHz (maximum) to measure the raw data in ASCII-SxP-format. The raw measurement data has been read out and processed on an external computer. A four-port RRMT-procedure was implemented in Matlab.

Fig. 5 shows the top-view of a used differential thru-standard and the dual |Z|-probes, manufactured by SUSS MicroTec.

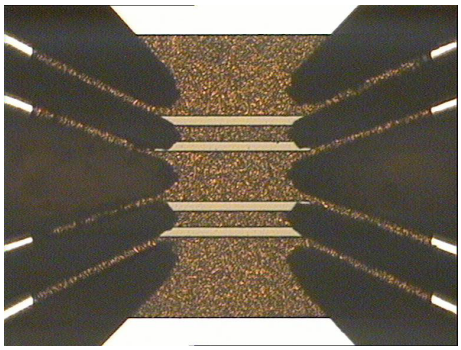

Fig. 5. On-wafer calibration standard for differential thru

Fig. 6 outlines a similar substrate to the one we used.

Fig. 7 shows the full set-up we used including the SUSS PA200HF Probe Station.

The first example for self-monitoring values of the RRMT is given in Fig. 8 with an illustration of the self-calibration results of the short-standard.

However, this and some other figures show a measurement error at 3 GHz. This error was caused by the test-set of the used network analyzer.

[11]The Ballmann network analyzer family S20X is based on a X-reflectometer. We used an 8-port network analyzer.

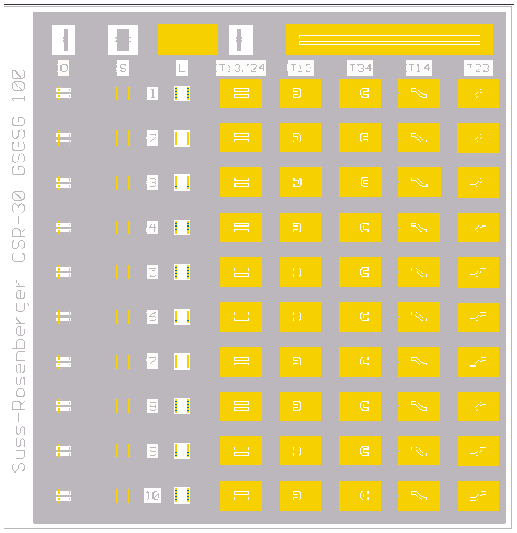

Fig. 6. On-wafer calibration and verification substrate

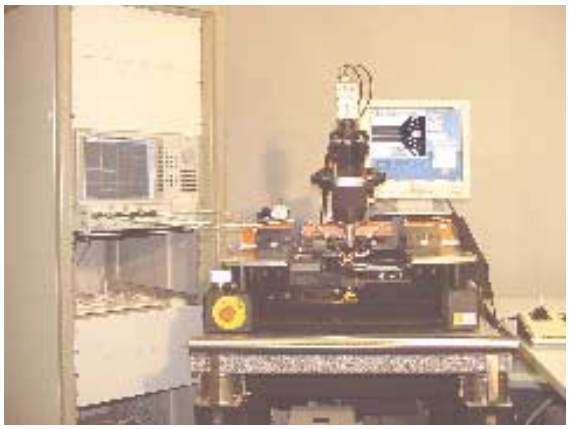

Fig. 7. Set-up for the on-wafer measurements

Fig. 9 shows the self-monitoring values of the open-standard calculated from the self-calibration process of the RRMT-procedure.

Both self-calibration results indicate that the set-up and self-calibration process works excellently.

The following results are error-corrected four-port RRMT-measurements.

However, a long matched transmission line with an open end is a very hard test (so-called ripple test) for a network analyzer set-up. Positive results of the magnitude at port 4 (Fig. 10) illustrate once more the robustness of the RRMT-procedure.

Also, the reflection value of a long matched line is a good proportion for verfication. Fig. 11 shows that the results are better than -30 dB.

The last measurement results in Fig. 12 illustrate the very accurate measurement performance of the RRMT-multiport procedure for transmission measurements. The results of a long line connected between port 1 and 4 were calculated by using the four-port RRMT-method.

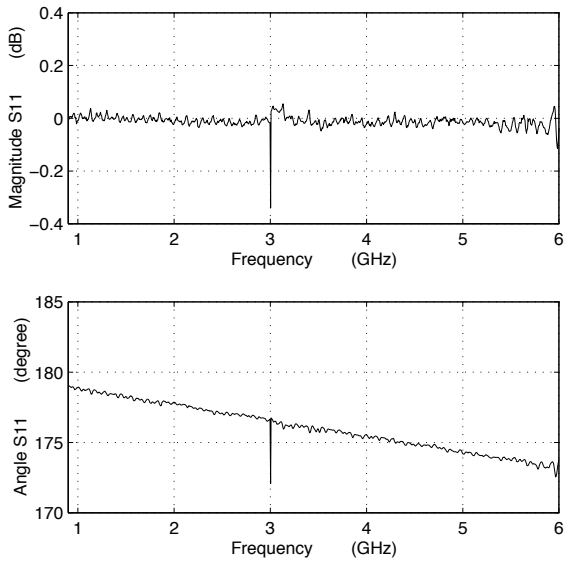

Fig. 8. RRMT-results in magnitude and phase of the self-calibration part for short-standard

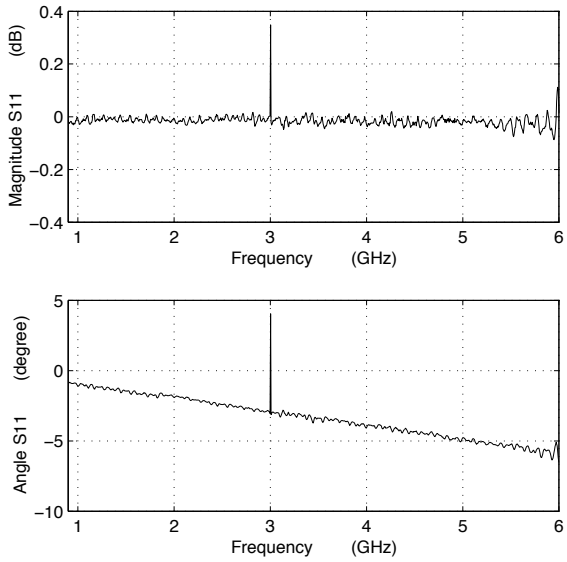

Fig. 9. RRMT-results in magnitude and phase of the self-calibration part for open-standard

VII. Conclusion

In this paper, advanced RF-techniques to perform accurate RF-on-wafer multiport measurements were presented. A large number of multiport calibration procedures can be designed. Two of them were derived and compared regarding the on-wafer conditions. A comparison was done with experimental measurements. The results clearly demonstrated proof of the advantages of the new multiport RRMT calibration procedure.

Acknowledgment

The authors are grateful to Mr. Ballmann, who provided the multiport network analyzer S208.

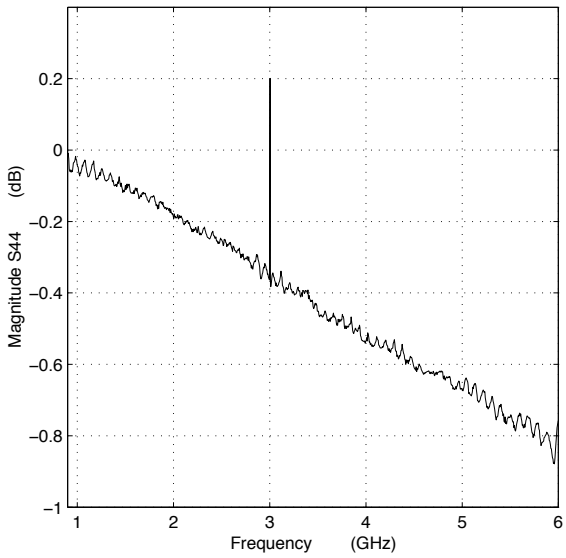

Fig. 10. Magnitude of RRMT error corrected measurement results of a long matched transmission line with an open end, connected at port 4

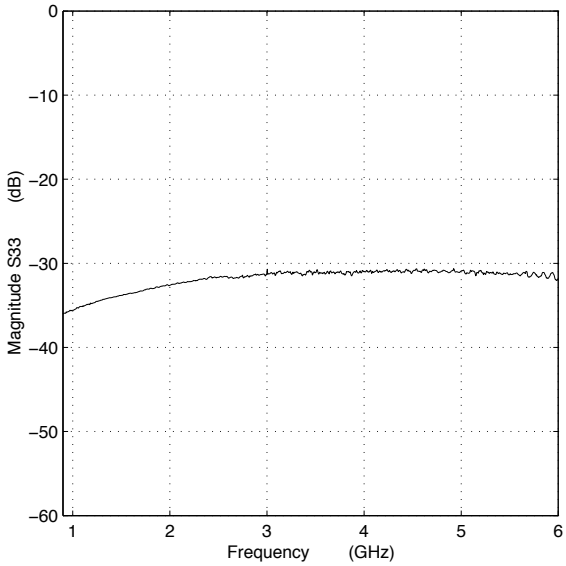

Fig. 11. Magnitude of RRMT error corrected reflection measurement results of a long transmission line, connected between port 3

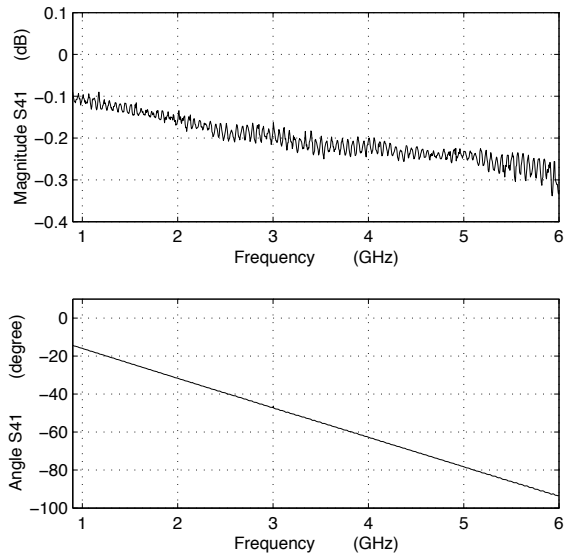

Fig. 12. Magnitude and phase of RRMT error corrected measurement results of a long transmission line, connected between port 1 and port 4

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13.3 Paper [54]: ”A robust broadband calibration method for wafer-level characterization of multiport devices”

A. Rumiantsev, H. Heuermann, and S. Schott, "A robust broadband calibration method for wafer-level characterization of multiport devices," in *ARFTG Microwave Measurements Conference-Spring, 69th*, 2007, pp. 56-60.

This paper described the theory and practical results of the new multiport calibration procedure especially suited for wafer-level device characterization over a wide frequency range. An analysis of the currently available multiport calibration approaches was carried out. The advantages and drawbacks of each approach were demonstrated. It was shown that a robust wafer-level multiport calibration procedure should combine the strengths of both 7-term and 10-term based algorithms. Corresponding to these requirements, the definition of the advanced multiport RRMT+ algorithm was given. The results of a practical experiment proved the theory and demonstrated the advantages of the new multiport RRMT+ calibration procedure.

For this paper, I planned the entire work, derived the mathematical solution, acquired measurement results, did the calculations and wrote the paper. My two co-authors, Prof. Holger Heuermann (Fachhochschule Aachen, Germany) and Steffen Schott (SUSS MicroTec, Germany) provided scientific and management supervision respectively.

A Robust Broadband Calibration Method for Wafer-Level Characterization of Multiport Devices

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***Abstract* — This paper describes the theory and practical results of the new multiport calibration procedure especially suited for wafer-level device characterization over a wide frequency range. An analysis of the currently available multiport calibration approaches was carried out. The advantages and drawbacks of each approach are demonstrated. It is shown that a robust wafer-level multiport calibration procedure should combine the strengths of both 7-term and 10-term based algorithms. It should also provide reference-match measurements on each VNA measurement port and be insensitive to the behavior of highly-reflective standards and the design of transmission standards.**

Corresponding to these requirements, the definition of the advanced multiport RRMT+ algorithm is given. The results of a practical experiment proved the theory and demonstrated the advantages of the new multiport RRMT+ calibration procedure.

***Index Terms* — multiport calibration, error correction, scattering parameters measurement.**

I. Introduction

The progress in wireless technologies and high-frequency broadband applications, the requirements for low power consumption, reduced electro-magnetic interferences, increased sensitivity, and data transfer rates drive the development of high-frequency, multiport mono- and mixed-mode devices, and thus improvement of multiport measurement systems.

As an example, the first 4-port 40 GHz vector network analyzer (VNA) based on a true 2*n*-receivers concept has been recently reported [1]. The hybrid multiport systems already provide 4-port measurement capability up to 67 GHz [2, 3]. The expansion of the frequency range of multiport VNAs requires new approaches for their calibration, particularly for wafer-level applications.

Many different calibration procedures were developed and implemented in commercial VNAs in the past. These can be separated into two groups based on the 10-term or 7-term model. 10-term approaches can be used for low-end VNAs (with *n*+1 measurement receivers, where *n* is number of VNA ports) and demonstrate the highest potential calibration dynamic range [4]. However, the requirement to have either ideal of fully known calibration standards significantly limits the application of these procedures. Therefore, it is not recommended to use 10-term based calibrations for wafer-level measurements beyond 20 GHz.

Many 7-term procedures are not sensitive to the non-ideal calibration standards short and open. Variants of these procedures (such as 2-port and multiport TRL[1], LRM[2], SOLR[3], LRM+[4], or TXX for general) are widely used for the calibration of broadband wafer-level measurement systems [5-8, 10, 12-14,]. However, as it was reported in [10], potential limitation of the calibration dynamic range of the 7-term-based methods may reduce the measurement accuracy, especially for differential devices under high-rejection conditions.

Additionally, multiport TXX-procedures may lead to significant calibration errors in the following cases (typical for many wafer-level setups):

- partly-known reflection (R) standards are not symmetrical (for instance, when measuring at a packaged-level);
- the rectangle, loop-back, or cross-over thru (Fig. 1) introduces a resonance at certain frequencies within the measurement range;
- the open, short, and load standards are not ideal or insufficiently modeled (for SOLR-like procedures)
- the load standard is not purely resistive and its impedance is frequency dependent;
- the load impedance is asymmetrical;

Fig. 1. Configuration of thru standards for a 4-port wafer-level calibration: straight thrus (port 1 – port 2, port 3 – port 4), loop-back thrus (port 1 – port 3, port 2 – port 4), cross-over thrus (port 1 – port 4, port 2 – port 3).

[1] Thru-Reflect-Line
[2] Line-Reflect-Match
[3] Short-Open-Load-Reciprocal
[4] Advanced Line-Reflect-Match

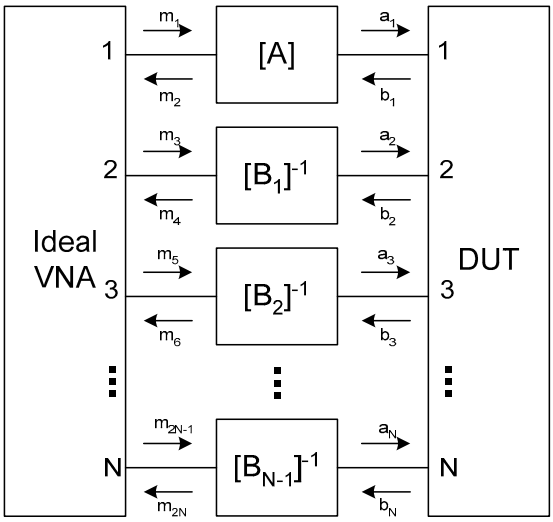

Fig. 2. Block diagram of *n*-port VNA that represents the ideal VNA, the matrices of error terms [*A*] and [B_i], and the DUT.

Therefore, it is necessary to develop a new multiport calibration procedure that will be free of the mentioned limitations.

The next chapter of this paper briefly describes the multiport measurement system and discusses different calibration approaches. Then, the novel generalized RRMT+ is introduced and experimental results verifying the application of this method are presented.

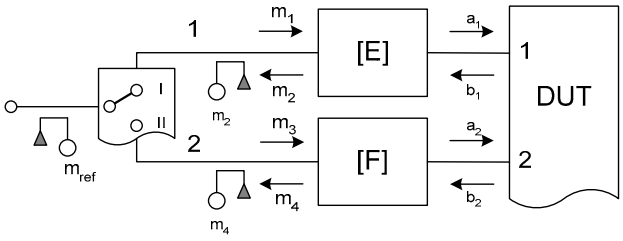

Fig. 3. Block diagram of the *n*-port VNA based on the reference channel architecture. For simplification, the diagram is reduced to its 2-port part. It shows the reference receiver m_{ref}, the signal source switch, the measurement receivers m_2 and m_4, and the 10-term model error matrices [*E*] and [*F*].

II. The Theory of the Generalized RRMT+

A. Multiport System

A multiport VNA can be described in general as shown in Fig. 2. The schematic diagram consists of an ideal VNA, the matrices [*A*], [B_i] of systematic measurement errors, and the DUT. An example of an *n*-port VNA with a reference channel architecture (with *n*+1 measurement receivers) is given in Fig. 3. Its error model is based on the 10-term representation: for every state of the system switch, 5 error terms can be defined for each pair of VNA ports. For instance, the two-port case gives terms: E_D^I, E_R^I, E_S^I, F_L^I, and F_T^I for the first state of the switch; and F_D^{II}, F_R^{II}, F_S^{II}, E_L^{II}, and E_T^{II}, for the second state of the switch (Fig. 4). Introducing matrices [*G*], [*H*], and so on, this description can easily be extended to the n-port case with $2*n^2+n$ error coefficients.

The multiport reflectometer VNA can be described by both the 10-term and the 7-term based models. The 7-term based *n*-port VNA error models consists of the $4*(n-1)+3$ coefficients.

Crosstalk between calibrating ports is not addressed in these models. Crosstalk affected systems require more sufficient modeling and include additional error terms.

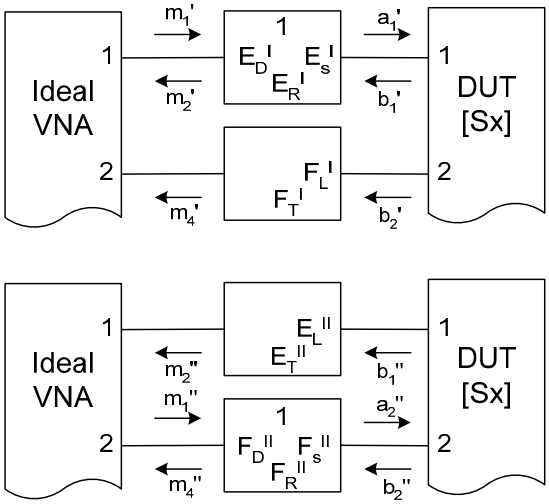

Fig. 4. Block diagram of a 2-port VNA described by the 10-term model for the first and second state of the switch.

It is easy to demonstrate that the relationship between the matrix [*M*] of measured parameters m_i and the DUT's actual parameters [*Sx*] can be represented over error-matrixes [*A*], [B_i], (or [*E*], [*F*], [*G*], etc.) in a similar way for both types of the *n*-port VNA realization [10, 11]. Once the measured values m_j as well as the coefficients of [*A*] and [B_k] (or [*E*], [*F*], etc.) are known (where j=1, 2, …, $2*n$, k=1, 2, …, n-1, and n is the number of the VNA ports), the actual *S*-parameters [*Sx*] of the unknown DUT can easily be found [e.g. 10].

B. Generalized RRMT+ Calibration Procedure

The fact that both 10-term and 7-term system descriptions can be applied to the multiport reflectometer VNA, gives the user enough flexibility in choosing an appropriate calibration procedure that fits to the measurement system applications in the best way possible. Since the 7-term calibration procedures

are not sensitive to inaccurate reflection calibration standards, they are used more often.

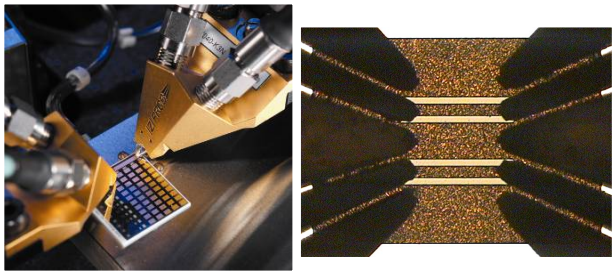

Fig. 5. Configuration of a 4-port wafer-level measurement and calibration: two Dual |**Z**| Probes and a differential (dual) straight calibration thru standard.

Calibrating the 7-term system, some selected error terms can be calculated by different variants of the TXX calibration within a single procedure: for instance, combining LRM and SOLR (a "hybrid calibration") [14, 15]. This approach has benefits when some thru standards are difficult to characterize (e.g. at wafer level). However, hybrid calibrations are neither free of possible "port bracing" nor the limitation of the calibration dynamic range because they are based on the 7-term model [10].

The novel RRMT+[5] multiport calibration approach is free from these limitations as well as from drawbacks discussed in the introduction. RRMT+ integrates the advantages of the 10-term and 7-term calibration algorithms into one procedure and extends the algorithm reported in [11, 16] for non-ideal thru standards.

In contrast to hybrid calibrations, the RRMT+ procedure uses the 7-term-based self-calibration process to calculate the accurate behavior of partly know standards (reflects and thrus) and the 10-term process to calibrate the system. Reflect standards (partly-known open and short) are characterized by the very robust LRM+ method [8]; reciprocal thrus (loop-back, cross-over, Fig. 1) are defined with the help of the SOLR algorithm [5]. Additionally, introducing at least one straight line in the measurements allows the characteristic impedance Z_0, phase, and attenuation constants of the straight thru to be found [17]. If necessary, the load can be specified.

Once all calibration standards are fully known, all error terms are calculated by the modified GSOLT procedure with non-ideal, but know standards [11]. Therefore the limitations of the multiport 10-term (SOLT), multiport 7-term (TXX) conventional and hybrid methods are overcome in one procedure.

C. RRMT+ Requirements for Calibration Standards

Depending on the number of DUT ports and their design, different configurations of the wafer-level measurement system are possible. For example, Fig. 5 shows two dual wafer probes with the same pitch. Calibrating the system like this, the set reflection (open, short, load) and transmission (thru, lines) standards can be measured. Reflection standards are typically grouped into one element consisting of four same-type standards. Thus, all required S-parameters (return loss) can be obtained after just one movement and contact. All elements in this group are equal to each other.

Full 4-port calibration requires 6 thru standards, as shown in Fig. 1. However, the electrical characteristics of only 3 standards are required: straight (port 1 – port 2), loop back (port 1 – port 3), and cross over (port 1 – port 4). The others are symmetrical.

Therefore, RRMT+ requires at minimum that:

1. open and short for all four ports are partly known (only within +/- π/2 their phase);
2. load port 1 and port 2 (or port 3 and port 4) are known, but they can be represented by any impedance element and different from each other;
3. straight thru port 1 – port 2 (or port 3 – port 4) is known.

Alternatively, requirements 2 and 3 can be replaced by adding an additional straight line with known physical length.

These requirements can vary depending on the system configuration and application type.

III. Experimental Results

The theory of the novel RRMT+ calibration approach was proven by experimental results. The experimental setup included a Rohde and Schwarz 40 GHz 4-port ZVA network analyzer; the semiautomatic PA200 probe system, the Dual |**Z**| Probe 500 µm pitch GSGSG configuration, and the GSGSG CSR-34 calibration substrate from SUSS MicroTec. Some additional test devices were used for the calibration comparison and calibration accuracy verification.

It is important to note that the probes and standards included in this setup had a very large pitch (500 µm). This presents a significant challenge for accurate broadband calibration (beyond 20 GHz).

To avoid the influence from contact repeatability error, the measured data were acquired in one measurement series in raw format and saved to an external PC. The calibration and the error correction were performed offline with the help of SussCal Professional calibration software[6].

The experimental results demonstrated a significant improvement in the measurement accuracy when the new RRMT+ calibration algorithm was used (Fig. 6-8).

[5] Advanced Reflect-Reflect-Match-Thru

[6] Available from SUSS MicroTec.

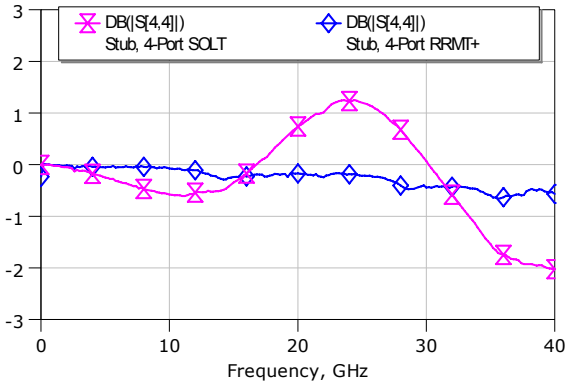

Fig. 6. Return loss measurements of the dual 6000 µm stub line on port 4 with respect to the 4-port SOLT and 4-port RRMT+ calibrations.

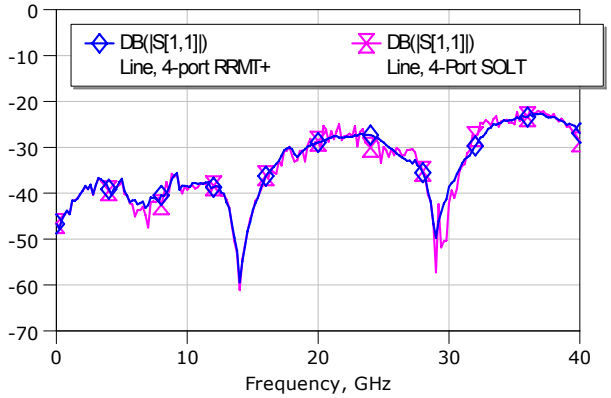

Fig. 7. Return loss measurements of the dual 6000 µm line on port 1 with respect to the 4-port SOLT and 4-port RRMT+ calibrations.

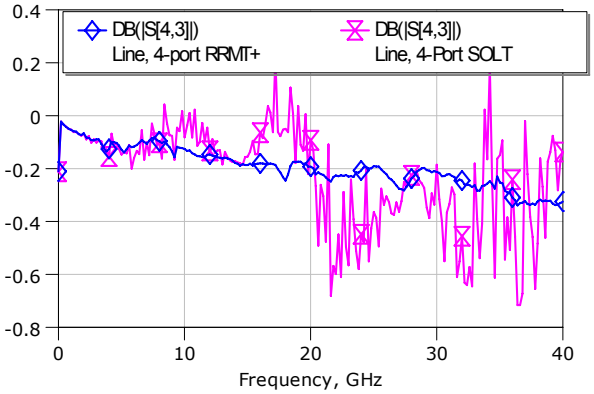

Fig. 8. Insertion loss measurements of the dual 6000 µm line between port 3 and port 4 with respect to the 4-port SOLT and 4-port RRMT+ calibrations.

IV. Conclusion

The analysis of conventional multiport calibration procedures was fulfilled. Their advantages and drawbacks for wafer-level applications were discussed and the novel RRMT+ calibration procedure was introduced.

It was demonstrated that the RRMT+ approach is not sensitive to conventional wafer-level multiport calibration problems: in general, it does not require accurate modeling of all reflection and transmission standards. This fact guarantees that the RRMT+ method is significantly less sensitive to typical calibration problems in a multiport wafer-level setup. Thus it is ideal for broadband characterization of multiport and differential devices without limitations of their sizes, frequency and design.

Acknowledgement

The authors wish to acknowledge excellent assistance and support of Frieder Simon, Christian Evers, and Klaus Beister of Rohde and Schwarz for providing the 40 GHz 4-port ZVA used for this experiment.

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14 ATTACHMENT TO CHAPTER 5

14.1 Paper [77]: “Applying the calibration comparison technique for verification of transmission line standards on silicon up to 110 GHz”

A. Rumiantsev, P. L. Corson, S. L. Sweeney, and U. Arz, "Applying the calibration comparison technique for verification of transmission line standards on silicon up to 110 GHz," in *ARFTG Microwave Measurements Conference-Spring, 73rd*, Boston, MA, 2009, pp. 1-6.

This paper presented the results of extracting the electrical characteristics of planar lines using the calibration comparison method for standards realized in IBM’s advanced 0.13 µm RF CMOS 8SF process. For the first time, this method was applied to characterizing the customized standards on silicon up to 110 GHz. Additionally, this paper considered the influences of the reference benchmark calibration standards, on the characterization accuracy of silicon wafer-embedded lines at mm-wave frequencies.

Here, I developed the entire verification methodology, did all calculations (except extraction of the DUT parameters), and wrote the major part of the conference paper. The design of the custom calibration standards, the electromagnetic simulations and the acquisition of measurement data and the extraction of the DUT parameters were done by Philip Corson and Susan Sweeney from IBM Microelectronics (Essex Junction, VT, USA). The analysis of the results was performed together with all co-authors, including Uwe Arz from Physikalisch-Technische Bundesanstalt (PTB) (Braunschweig, Germany).

Applying the Calibration Comparison Technique for Verification of Transmission Line Standards on Silicon up to 110 GHz

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***Abstract* — This paper will present the results of extracting the electrical characteristics of planar lines using the calibration comparison method for standards realized in IBM's advanced 0.13 µm CMOS process. For the first time, this method is applied to characterizing the customized standards on silicon up to 110 GHz. Additionally, this paper considers the influences of the reference benchmark calibration standards, included with GaAs reference material RM8130, on the characterization accuracy of silicon wafer-embedded lines at mm-wave frequencies.**

I. Introduction

Accurate on-wafer measurement of high frequency scattering (S-) parameters have already become an essential step of characterizing devices used in high frequency applications, such as advanced communications circuits. As technology scaling advances and device performance increases, it is becoming essential to improve the calibration and ultimately the measurement accuracy of an on-wafer S-parameter characterization system. Accurate on-wafer network analyzer calibration and establishment of the measurement reference plane close to the wafer-embedded device under test (DUT) at mm-wave frequencies is now necessary, reducing the reliance on inaccurate de-embedding methods of the probe padset parasitics.

The multiline TRL[1] calibration [1] procedure together with methods for characterizing planar lines [2, 3] developed by the National Institute of Standards and Technology (NIST) has already established a solid reference in the on-wafer calibrations for semi-insulating wafers. However, even more challenging and urgently required, is the application of these techniques and the analysis of their accuracy for semi-conductive wafers [4].

A great variety of fabrication techniques complicates the task of specifying and verifying planar calibrations. Research undertaken by NIST provided a procedure for comparing wafer-level calibrations, identifying setup drift, as well as verifying calibration standards [5]. Furthermore, the calibration comparison procedure can be successfully used to characterize the electrical properties of unknown standards on alumina [6] as well as on silicon [7-9]. However, to the author's knowledge, this method has not been verified yet for characterizing calibration standards on lossy substrates above 50 GHz.

[1] Thru-Reflect-Line

This paper will present the results of extracting the electrical characteristics of planar lines using the calibration comparison method for standards realized in an IBM advanced 0.13 µm CMOS process. For the first time, this method is applied to characterize customized standards on silicon up to 110 GHz. Additionally, this paper considers the influences of wafer probes and the reference benchmark calibration standards on the characterization accuracy of lines on silicon.

II. On-Wafer Calibration Standards and Characterization Methods

A. Calibration Standard on Silicon

The experimental calibration set included all standards required for the multiline TRL calibration (with three lines). Standards were fabricated within a typical 2-port GSG on-wafer probe padset. The ground pads, signal pad, and signal launch lines were placed on an upper metal level layer, while a meshed ground plane is placed under the signal geometries on the first metal level layer. The transmission lines were fabricated as extensions of the signal launch lines. The line design addresses the specifics of the bulk CMOS process. Line lengths were adjusted to cover a frequency band from 1 GHz to 110 GHz. The test set included various lumped standards, such as Load, and different Open and Short elements.

Three different techniques were applied to characterize the electrical properties of the test set lines: the lumped load method, the calibration comparison method, and EM simulations.

B. Lumped Load Method

The lumped load method was originally introduced in [3]. It extracts the characteristic impedance Z_0 of a quasi-TEM line fabricated on a semi-insulating substrate from its measured capacitance per unit length C in three steps. First, the multiline TRL calibration is performed with the examined lines setting the calibration reference impedance Z_r to the characteristic impedance of the line Z_l. Second, the reflection coefficient Γ_{load} and the DC resistance $R_{load.dc}$ of a reference load element are measured. Finally, the line capacitance is calculated from:

$$C\left[1 - j\frac{G}{\omega C}\right] \approx \frac{\gamma}{j\omega R_{load.dc}}\frac{1+\Gamma_{load}}{1-\Gamma_{load}} \qquad (1)$$

where: γ is the line propagation constant, measured from the multiline TRL calibration.

C. Calibration Comparison Method

The calibration comparison method described in [8] relies on a two-tier calibration process. The first-tier calibration is performed in a set of well-defined reference lines. In this calibration, the system reference impedance Z_r is set to 50 Ω, and the position of the measurement reference plane is moved to the probe tips. The second-tier calibration is performed in the transmission lines one wishes to characterize. Here, the reference plane is also set to the probe tips. The calibration comparison procedure yields error boxes that can be modeled by a simple equivalent circuit. Finally, a robust estimate of the measured line's characteristic impedance can be derived, which is insensitive to the contact pad parasitics.

D. EM Simulation

The thru line was simulated with a simplified model using the 3D full-wave electromagnetic field simulation package Ansoft HFSS®[4]. The 3D structure included all the passivation and metal layers with interconnects simplified to solid bars. Simulation results yield the electrical parameters of the transmission line including gamma and the characteristic impedance.

III. Measurement Setup

The experimental setup included an Agilent 8510XF VNA, a semi-automatic wafer-probe station, and 110 GHz wafer probe tips with a pitch of 100 µm. To establish a reference calibration, two different sets of standards were used: a semi-insulating GaAs reference material 8130[2] (RM8130), and a commercially available alumina calibration substrate recommended by its vendor for application up to 110 GHz.

Measurement data from the VNA were recorded with SussCal®[3]. Off-line calibration, error correction, calibration comparison, and the line parameter extraction were performed using MultiCal©, LINEPAR, CAP, and ExtractZo from NIST.

A. Reference Material RM8130

The RM8130 consists of a coplanar wave guide (CPW) multiline TRL calibration set: a 550 µm long thru line, five lines with lengths of 2685 µm, 3750 µm, 7115 µm, 20245 µm, and 40550 µm, and two offset shorts located at a distance of 225 µm from the beginning of the line. Additionally, there are 12 verification reference elements.

According to the individual test results provided by NIST for each RM8130, the actual line capacitance of RM CPW line used for this investigation is 1.7877 pF/cm. This value is used by the benchmark multiline TRL calibration for the accurate definition of the characteristic impedance of the RM8130 lines and the transformation of the measurement system reference impedance to 50 . RM8130 is only specified for use up to 40 GHz [10].

B. Alumina Calibration Substrate

The alumina calibration substrate consists of lumped standards (open, short, and load) as well as CPW line sets: a 150 µm long thru line, four lines with lengths of 6550 µm, 1450 µm, 950 µm, and 500 µm. Its estimated effective dielectric constant is about 5.26. The substrate is 625 µm thick.

The CPW lines of the alumina calibration substrate are not characterized by the vendor. Thus, the line characteristic impedance and the propagation constant must be computed for the alumina benchmark probe tip calibration [6].

We supposed that the measured characteristics of alumina CPW lines can vary significantly due to two factors: the fabrication tolerances of the lines and the influence of different probe tip design. Thus, we measured two alumina substrates of the same type using two differently designed wafer probes.

IV. Experimental Results

A. Verification of CPW Lines from Alumina Substrate

The CPW lines from both alumina substrates were characterized by the lumped load and the calibration comparison method. For the lumped load method, the DC resistance of the load standard from each substrate was accurately measured. The line capacitance per unit length C was extracted from CAP program and the $G/(\ C)$ component was neglected. The effective dielectric constant was measured by the multiline TRL procedure and the line characteristic impedance Z_0 was extracted using the method of [2].

For the calibration comparison method, the first-tier benchmark multiline TRL was performed on the reference material RM8130. The reference plane was set to the probe tip end and the reference impedance was accurately transformed to 50 using the capacitance value of the RM lines as specified by NIST. The characteristic impedance Z_0 of the CPW lines on alumina was extracted from the second-tier multiline TRL error boxes with the help of the ExtractZo program. Finally, inductance L, resistance R, capacitance C, and conductance G per unit length of the alumina CPW lines were estimated from the LINEPAR program (Fig. 1).

Conductance G and resistance R per unit length extracted from both methods are in good agreement for both measured setups below 40 GHz. The variation of about 7% for the capacitance C and about 5% for the inductance L per unit length can be attributed to tolerances in the fabrication of the alumina substrates.

Fig. 1 also shows that the calibration comparison results strongly deviate above 40 GHz for both setups. This indicates the cross section of the RM8130 CPW lines was not optimized for frequencies above 40 GHz.

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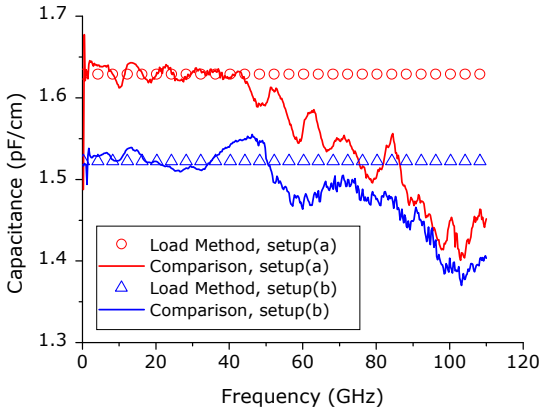
[2] Available from NIST

[3] SussCal is available from SUSS MicroTec.

[4] HFSS is commercially-available from ANSYS Inc.



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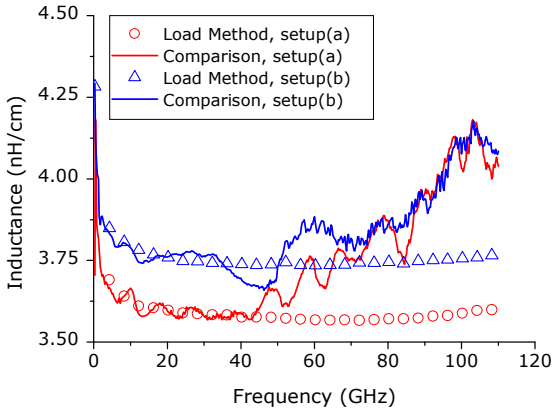
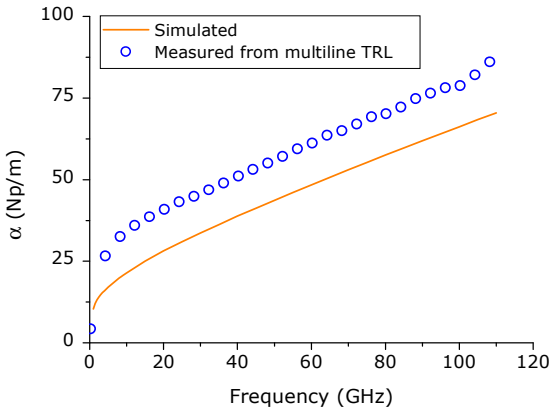
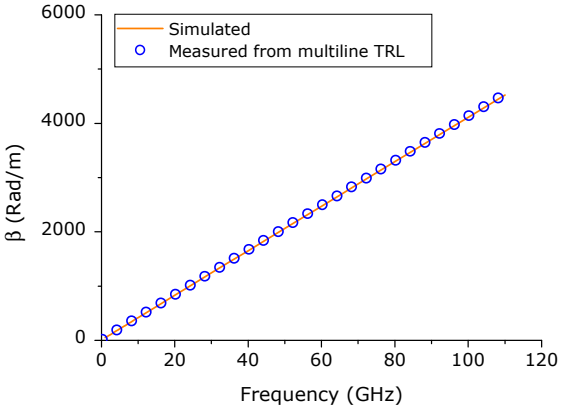


b)

Fig. 1. Parameters of the alumina CPW line extracted from the calibration comparison to the reference RM8130 calibration and the load method for two setups.



a)



b)

Fig. 2. Simulated and measured attenuation (a) and phase (b) constants of examined silicon line.

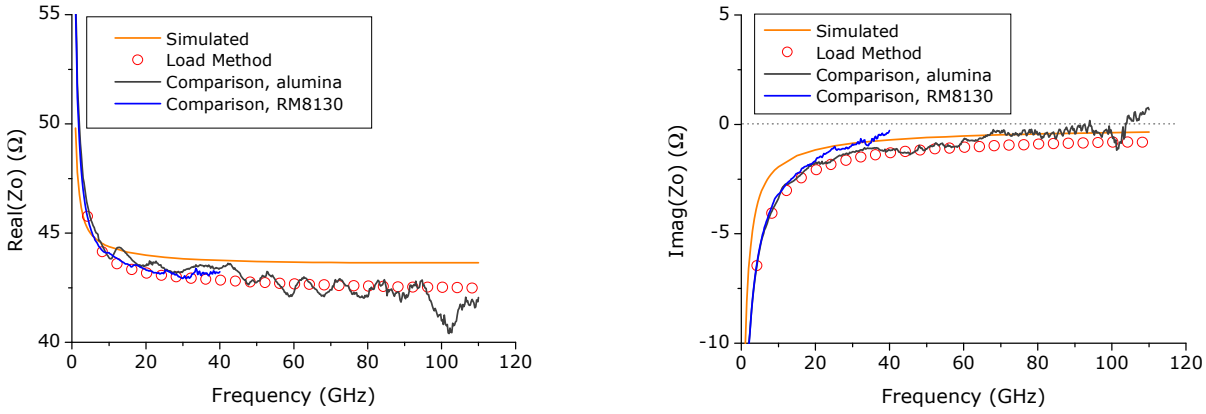
Comparing results for the conductances per unit length of both methods up to 40 GHz, we concluded that the evaluated alumina CPW lines have negligible transverse losses.

B. Lines on Silicon

The propagation constant of the examined lines on silicon was measured using multiline TRL and compared to the simulation result (Fig. 2). The line characteristic impedance Z_0 was extracted from three approaches: calibration comparison method referenced to the RM8130 (up to 40 GHz), calibration comparison method referenced to alumina substrate (up to 110 GHz), and the lumped load method (up to 110 GHz), as shown in Fig. 3. From the results obtained (Fig. 4), line capacitance C, inductance L per unit length as well as coefficients $G/(C)$ and $L/(R)$ were calculated. Fig. 4, c) shows the transverse losses of the silicon lines used in this study can be neglected.

C. Extraction of DUT Parameters

An on-wafer NFET transistor, with a channel length of 0.12 µm for which the wiring to the transistor was carefully designed to be consistent with the on-wafer calibration standards, was also measured. The raw, uncalibrated measured data were corrected to a calibration reference plane occurring in the middle of the via stack at the end of the signal launch line of the probe padset, as shown in [4]. A small amount of parasitics remaining after calibration, occurring between the calibration reference plane and the device, were de-embedded using standard Open-Short de-embedding methods.



a) b)

Fig. 3. Simulated and extracted real (a) and imaginary (b) parts of the examined silicon line characteristic impedance Z_0. Extracted data were obtained from the load method and the calibration comparison method to reference material RM8130 and alumina substrate. Comparison to RM8130 is limited in frequency to 40 GHz due specification of the reference material used.

Figure 5 shows the extracted drain-to-gate capacitance versus frequency for the transistor. In addition to the excellent flatness versus frequency, the data also shows very little variation and sensitivity to the difference in the various methods of extracting the electrical characteristics of the calibration standards.

V. Discussion

Both the calibration comparison method and the lumped load method have proven to be valid methods for extracting the electrical characteristics of planar transmission line standards. From Fig. 1 we conclude that the use of the NIST RM8130 cannot be recommended above 40 GHz. However, at low frequencies the calibration comparison method using the RM is in good agreement with the lumped load method. Furthermore, as shown in Fig. 3 and Fig. 4, both methods are in acceptable agreement up to 110 GHz. The difference in the substrate material between the GaAs of the RM, the alumina, and the silicon appears to be successfully compensated for in the calibration comparison method.

We observed slight rippling of the extracted parameters of alumina CPW lines (Fig. 1), as well as for the silicon lines measured with the respect to the first-tier reference calibration on alumina (Fig. 3 and Fig. 4). Possible reasons for such effects include the influence of the high-resistivity absorbing layer that extends under the ground conductors of the alumina CPW lines, non-ideal calibration boundary conditions, and the impact of the design of the wafer probes on the calibration standards characteristics [11]. Further detailed investigations of these phenomena are required.

As shown in Fig. 1, our results indicate that there are some fabrication variations (such as thickness, surface roughness and the roughness of the edges between ground and signal conductors, signal gap, and the substrate dielectric), or probe-type dependencies, in commercially offered alumina substrates. Therefore, in order to use the alumina substrate for reference calibrations, it is mandatory to characterize the electrical properties of the substrate together with the probes, using a well established benchmark calibration. This issue highlights the need for a reference material that is valid to 110 GHz. To the author's knowledge, such a reference material is not available yet.

Thus, the lumped load method of measuring line capacitance per unit length is currently recommended for alumina. Also, it was proven that the alumina CPW lines have negligible loss and the extraction of the coefficient $G/(\ C)$ is not needed.

Most importantly however, the lumped load method demonstrates acceptable accuracy for determining the electrical characteristics of the transmission line standards on silicon investigated here up to 110 GHz. The success shown in this study is attributable to the design of the line standards on the silicon. The first metal level ground plane under the signal provides a dominant microstrip propagation mode. This ground plane is common practice in the industry. Due to fabrication rules, the ground plane must be a mesh, and further studies are needed to evaluate the geometries where the microstrip mode dominates and the lumped load method is valid.

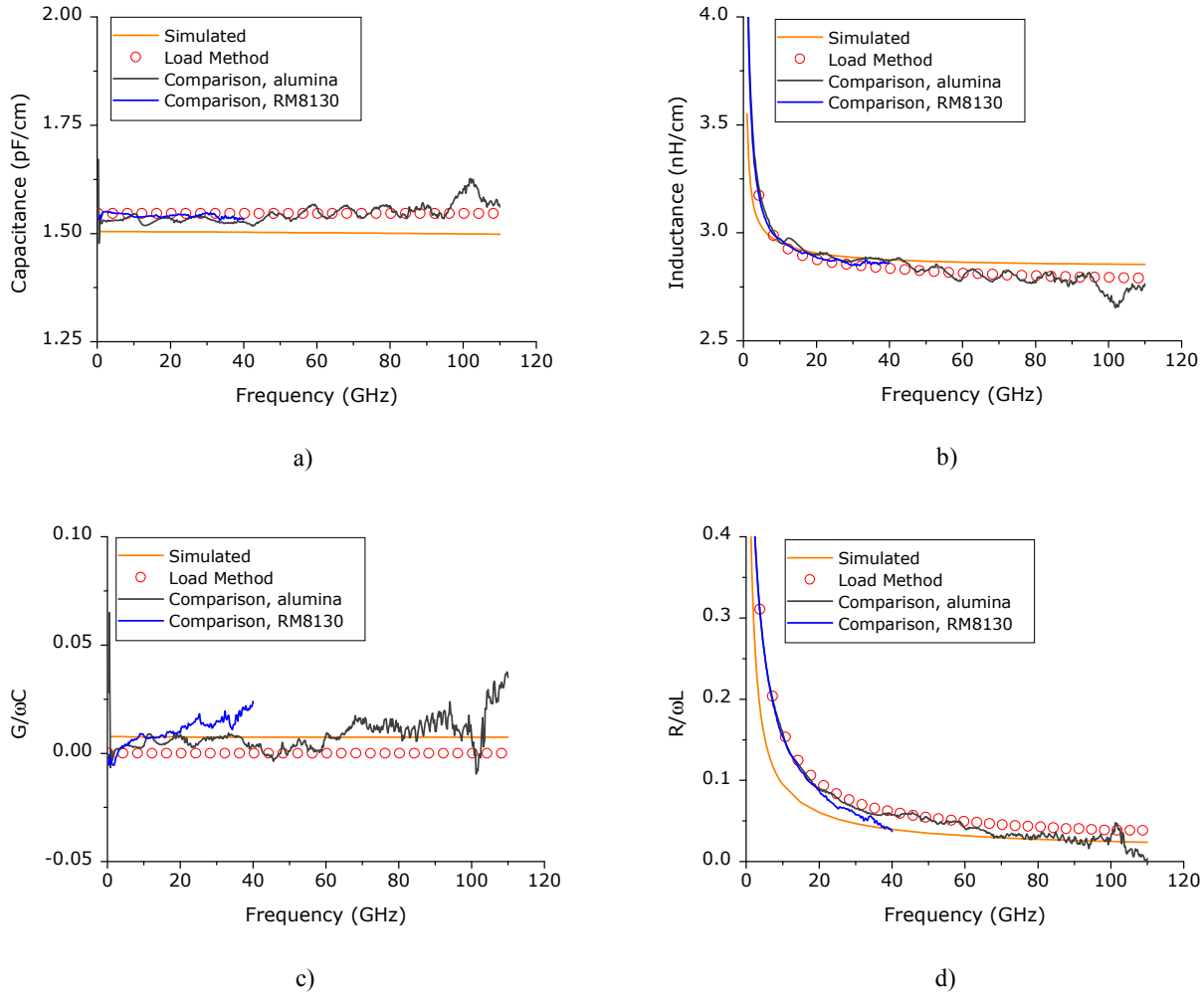


Fig. 4. Comparison of the simulated and extracted parameters of the examined silicon line. Parameters are extracted from the lumped load method as well as from the calibration comparison to the reference material RM8130 and alumina substrate. Comparison to RM8130 is limited in frequency to 40 GHz due specification of the reference material used.

Careful characterization of the thru and the load is essential for developing an accurate LRM-based on-wafer calibration method for use in silicon processes [4]. This work has shown successful characterization of the thru line, providing a basis for a successful LRM on-wafer calibration.

All three methods for determining the electrical characteristics of the calibration standards studied here, and using the resulting TRL calibration to correct the raw transistor measurements, are yielding tight agreement for extracted transistor parameters, as shown in Fig. 5. This result reveals the device insensitivity to the method of line standard characteristics extraction. In addition, it indicates that the successful development of an on-wafer calibration method on silicon for device measurement up to 110 GHz is possible.

VI. Conclusion

Summarizing, for the first time the calibration comparison method was applied to extract the electrical characteristics of planar CMOS lines up to 110 GHz. This was done using commercially available alumina calibration substrate, as well as the GaAs reference material RM8130. We demonstrated that commercially available calibration substrates can be used for characterizing customized standards on silicon at mm-wave frequencies with acceptable accuracy.

As a result, the implementation of wafer-embedded calibration techniques on lossy substrates at mm-wave frequencies, such as multiline TRL, can be significantly simplified. Thus, the required improvement in the

measurement accuracy of advanced RF CMOS components at frequencies up to 110 GHz can be achieved.

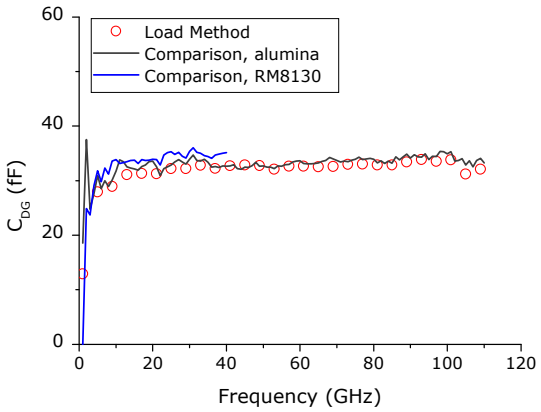


Fig. 5 Extracted drain-to-gate capacitance of a of 0.12 µm channel length NFET with respect to the load and calibration comparison methods.

ACKNOWLEDGMENT

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14.2 Paper [23]: “Calibration standards verification procedure using the calibration comparison technique”

A. Rumiantsev, R. Doerner, and S. Thies, "Calibration standards verification procedure using the calibration comparison technique," in *36th European Microwave Conference*, 2006, pp. 489-491.

This article examined the verification procedure of coplanar calibration standards based on the calibration comparison technique. For the first time, different commercially available alumina calibration substrates were compared using the NIST multiline TRL calibration procedure, calibration comparison approach, and the NIST GaAs CPW calibration reference material RM8130. The worst case error bounds for the measurement of passive devices compared to the reference multiline TRL on the RM8130 were calculated for each tested substrate.

This work was co-authored by Ralf Doerner from Ferdinand-Braun-Institut (FBH), Leibniz-Institut fuer Hoechstfrequenztechnik (Berlin, Germany) and Steffen Thies from Rosenberger (Fridolfing, Germany). For this work, I developed the verification methodology, planned the work, defined the measurement campaign, and wrote the conference paper. I did calculations and the data analysis together with Ralf Doerner. The measurement results were acquired by Ralf Doerner at FBH facility.

Calibration Standards Verification Procedure Using the Calibration Comparison Technique

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***Abstract* — This article examines the verification procedure of coplanar calibration standards based on the calibration comparison technique. For the first time, different commercially available alumina calibration substrates were compared using the NIST multiline TRL calibration procedure, calibration comparison approach, and the NIST GaAs CPW calibration reference material RM8130. The characteristic impedance of the verified calibration line standards is extracted using the multiline TRL procedure and the definition of the load standard resistance. The error circuit, describing difference of the substrate medium and the standard design is extracted. Finally, the worst case error bounds for the measurement of passive devices compared to the reference multiline TRL on the RM8130 are calculated for each tested substrate.**

***Index Terms* — calibration, error correction, calibration comparison, scattering parameters measurement.**

I. Introduction

Significant progress in modern 2.5- and 3-dimensional microwave simulation tools provides quick and accurate design and optimization of microwave components. However, variations in the fabrication process raise the necessity of the accurate post-production measurement and characterization. It is especially a problem for the CPW calibration standards: the design and fabrication process makes it impossible to trace the mechanical and electrical properties of the standards to the natural constants directly. The alternative verification approaches are still a challenge. The uncertainty introduced during the manufacturing of standards influences the accuracy of the calibration, and it can be used for indirectly verifying the standards.

The research undertaken by the National Institute of Standards and Technology (NIST) provided a technique for comparing different wafer-level calibrations to those performed by NIST, which have well-defined boundaries (the system reference impedance and the position of the measurement plane) [1]. This technique can be successfully used by industrial laboratories for calibration verification purposes, e.g. [2]. This paper presents the application and results of using the calibration comparison technique for verifying the accuracy of commercially-available CPW calibration standards.

II. Verification Procedure

The calibration comparison technique provides the worst-case deviations of the measured S-parameters of passive devices for the examined (first-tier) calibration with respect to the benchmark (second-tier) calibration. Deviations are treated as $|S_{ij}-S_{ij}'|$, for $ij \in \{11, 12, 21, 22\}$, where S_{ij}' is the S-parameter measured by the calibration to be tested, and S_{ij} is the S-parameter measured by the benchmark calibration. The deviations are calculated from the obtained error matrices or "error boxes" [A] and [B] (Fig. 1), and represent three sources of possible error: differing calibration methods, medium and launch geometries, and fabrication error. In the ideal case, both calibrations, benchmark and examined, are equal, [A] and [B] are unity matrices, and the error bounds $|S_{ij}-S_{ij}'|$ are zero.

Selecting the same calibration method for the first-tier and the second-tier calibration eliminates the first error source. Using the procedure outlined in [3], the error resulting from the difference of the medium and launch geometries for the reference and test calibration can be excluded. Finally, the error matrices [A] and [B] will quantitatively represent the fabrication uncertainty of the examined set of standards.

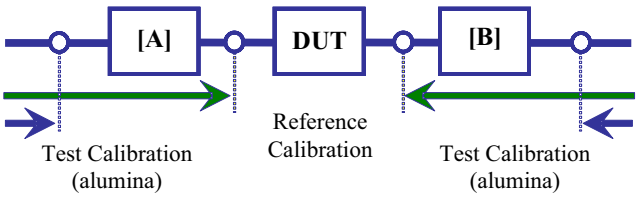

Fig. 1. The error matrixes [A] and [B] obtained by the calibration comparison method.

III. Experimental Results

For the independent evaluation, an experimental setup providing 110 GHz measurement capabilities was used. The setup for wafer-level measurements included an Agilent PNA 110 GHz network analyzer, a PM8 manual wafer-probe station from SUSS MicroTec, and 110 GHz wafer probe tips with a 125 µm pitch. The GaAs CPW lines (the reference material RM8130) fabricated and specified by NIST were used as a reference calibration set.

The integrity of the setup (Fig. 2) was verified and the measurement system drift within the experiment was defined acc. to [4] using the RM8130, the reference data, the multiline TRL calibration method, and the MultiCal® software package provided by NIST.

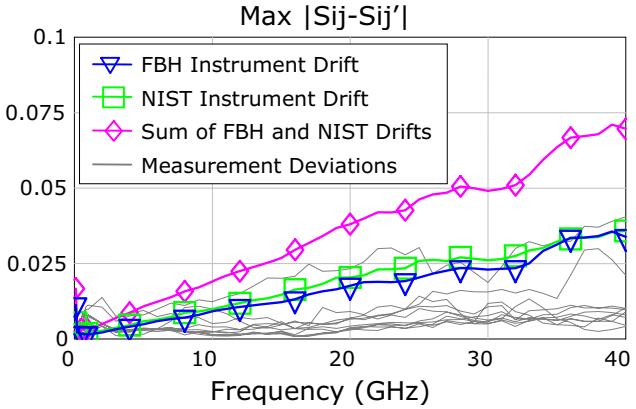

Fig. 2. Verification results on integrity of the 110 GHz wafer-level measurement setup used. Due to the frequency limitation of the reference data for the RM8130 provided by NIST, the results for the setup are limited to 40 GHz.

NIST multiline TRL [5] was selected as the calibration method. In conjunction with methods proposed in [6] and [7], this procedure allows accurate setting of the measurement system reference impedance to 50 Ohm as well as a precise definition of the measurement reference plane. To avoid additional uncertainty due to contact repeatability, all required data were acquired in one measurement series in raw-data format with the help of the calibration software SussCal®[1] and saved externally for further analysis.

If the characteristic impedance Z_0 and the physical length l are well known, a calibration based on the distributed standards (TRL-like) provides very accurate results [5]. Then, the lumped standards (Open, Short, and Load) can easily be specified [8]. Therefore, the characteristic impedance Z_0 of the alumina CPW lines was selected as verification criteria. The examined substrates were the commercially available from SUSS MicroTec CSR-3, CSR-8, and comparable substrate from another vendor (referenced further as the Sub A).

[1] Available from SUSS MicroTec.

It was found that the line Z_0 definition method based on the direct measurement of its capacitance C per unit length [6] of the alumina CPW lines does not provide the required accuracy. The commercially available alumina substrates typically have lines shorter then 7 mm. This significantly decreases the measurement accuracy of the line's C. Thus the found variation range of C was 1.651…1.337 pF/cm. It corresponds to the characteristic impedance Z_0 variation from 46.34 Ohm to 57.01 Ohm and demonstrates the significant measurement error.

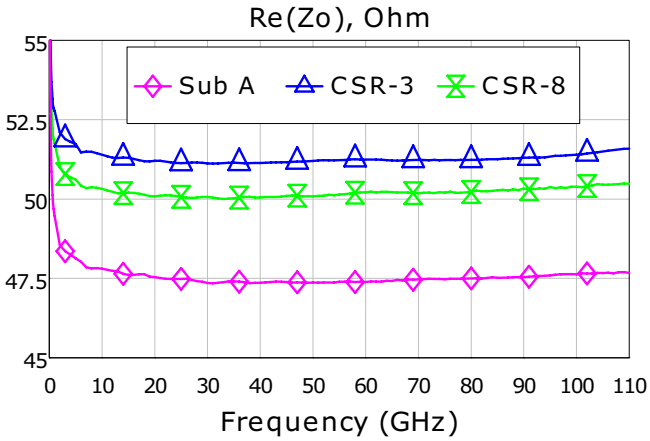

Fig. 3. Extracted value (real part) of the line characteristic impedance Z_0 for CSR-3, CSR-8, and Sub A calibration substrates.

Consequently, an alternative procedure was used to obtain the line capacitance C and, finally, the characteristic impedance Z_0 of the tested alumina lines. The resistance R of the load standard located on the same substrate was accurately measured using the 4-terminal method. Then, the first tier multiline TRL was performed setting the calibration reference impedance to the characteristic impedance Z_0 of the alumina lines used. The frequency range where the tested lines are no longer dispersive and, on the other hand, the load reactance is negligible was used to extract the value of the line capacitance C acc. to [6]. The procedure was repeated using other alumina substrates. The Table I shows the extracted values of the line capacitance C for each substrate respectively.

TABLE I
Extracted Line Capacitance

Substrate	C (pF/cm)
A	1.57
CSR-3	1.51
CSR-8	1.5

Based on the results, the reference plane of the examined calibration was accurately set to the probe tip end and the measurement reference impedance was transformed to 50 Ohm. The line characteristic impedance Z_0 was extracted

for each calibration substrate with the help of MultiCal® software package (Fig. 3).

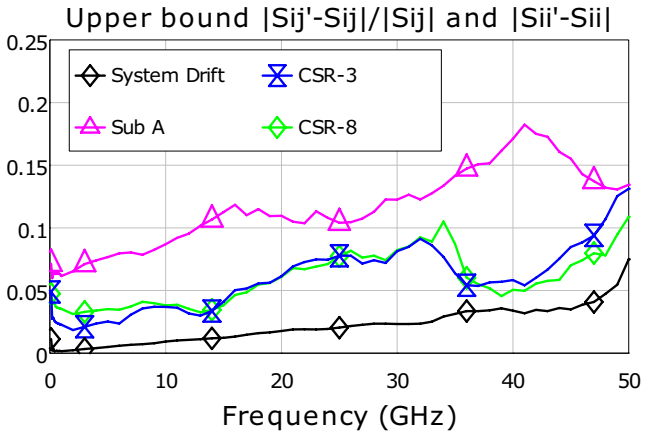

Fig. 4. Results of the accuracy verification for the multiline TRL calibration on CSR-3, CSR-8, and Sub A calibration substrates without correction for the line impedance.

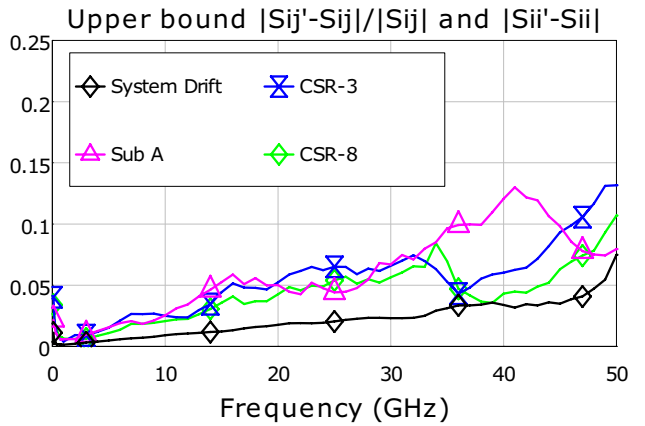

Fig. 5. Results of the accuracy verification for the multiline TRL calibration on CSR-3, CSR-8, and Sub A calibration substrates with correction for the line impedance.

The second-tier reference calibration was done. Results for tested alumina substrates are presented in Fig. 4 and Fig. 5 and validate the extraction method.

Finally, the same validation procedure was performed with the respect to the first-tier lumped LRM+ calibration [2] on each substrate proving its accuracy (Fig. 6).

IV. Conclusion

Different commercially available alumina calibration substrates were verified with the help of the calibration comparison procedure. The line characteristic impedance Z_0 was extracted. The found values are within tolerance of 3.6% for the CSR-3, 0.8% for the CSR-8, and 4.9% for the Sub A calibration substrates, respectively (for the frequency range of 10 GHz–110 GHz).

It has been demonstrated that the maximum error bound of 0.13 for the CSR-3, 0.11 for CSR-8, and 0.18 for the Sub A can be obtained up to 50 GHz. Obviously, additional correction techniques will be required to achieve the same results as for the CSR substrate family if the other commercially available alumina substrate is used.

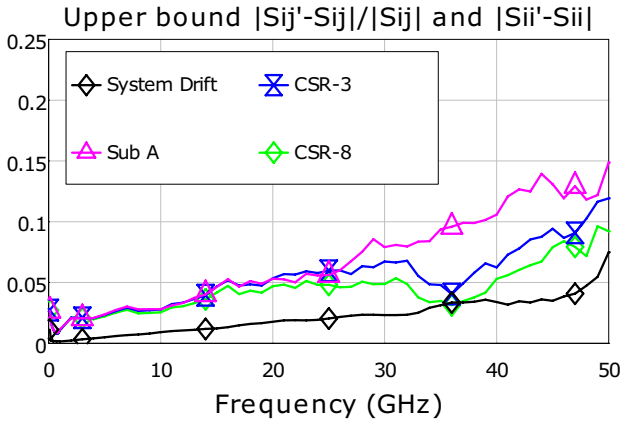

Fig. 6. Results of the accuracy verification for the LRM+ calibration procdure on CSR-3, CSR-8, and Sub A calibration substrates.

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15 ATTACHMENT TO CHAPTER 6

15.1 Paper [56]: “Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications"

A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," in *ARFTG Microwave Measurements Conference-Fall, 72nd*, pp. 132-135, 2008.

This paper presented a quantitative comparison of the reference multiline TRL and the transfer TMR for a customized set of standards in a CMOS process using IBM’s 0.13 µm technology. This comparison was undertaken for the first time and covered a frequency range from 1 GHz to 110 GHz. It was demonstrated that the accuracy of the on-wafer multiline TRL and the transfer TMR calibration were in very good agreement. Both methods outperformed the conventional off-wafer calibration with the DUT contact pad parasitics de-embedded.

For this paper, I planned the work, framed the design requirements to the transfer TMR standards, developed the accuracy verification method, did all offline calibration calculations and wrote related section of the paper. The standards were optimized, laid out, and measured by Philip Corson and Susan Sweeney from IBM Microelectronics (Essex Junction, VT, USA). Philip Corson provided EM simulation analysis. Susan Sweeney extracted the parameters of the test DUT. The analysis of the results was performed together with all co-authors.

Comparison of On-Wafer Multiline TRL and LRM+ Calibrations for RF CMOS Applications

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***Abstract* — This paper presents a quantitative comparison of the reference multiline TRL and LRM+ for a customized set of standards in a CMOS process using IBM's 0.13 µm technology. This comparison was undertaken for the first time and covered a frequency range from 1 to 110 GHz. It was demonstrated that the accuracy of the on-wafer multiline TRL and LRM+ calibration were in very good agreement. Both methods outperform the conventional off-wafer calibration with the DUT contact pad parasitics de-embedded.**

***Index Terms* — calibration, error correction, calibration comparison, scattering parameters measurement, CMOS, de-embedding.**

I. Introduction

As technology scaling advances and device performance increases, it is becoming essential to obtain accurate high frequency scattering parameters of on-wafer devices used in applications such as communications circuits. Accurate on-wafer network analyzer calibration and the establishment of the measurement reference plane close to the device under test (DUT) is now necessary to reduce the reliance on inaccurate de-embedding methods of the probe padset parasitics.

Today, the commonly-used method for calibrating a wafer-level measurement setup for RF CMOS application consists of two steps:

- Step 1: off-wafer calibration to the probe tip performed on a commercially-available alumina calibration substrate;
- Step 2: translation of the measurement reference plane to the DUT using contact pad de-embedding techniques.

Such an approach was introduced for the first time at the end of the 1980s [1]. This approach recommended using Open and Short elements as the RF de-embedding test structures. This method provided a reasonable alternative to the on-wafer calibration challenges for silicon at that time, in contrast to the high-frequency GaAs applications [2]. Method [1] required neither a perfectly matched load nor the calibration lines embedded on the test chip.

However, further improvement of RF CMOS device performance and increasing operation frequencies to 110 GHz and beyond requires improved measurement accuracy. The de-embedding procedure has become more and more complicated [3, 4], and finally, the need to de-embed the load element has been reported [5, 6].

This work is a further development of wafer-level calibration techniques with a customized set of lumped standards for mm-wave frequency applications. The earlier investigations reported in [7] demonstrated implementation of a lumped LRM+[1] calibration methodology on a conductive (SiGe:C) wafer up to 110 GHz. However, results presented in [7] verify the calibration accuracy qualitatively, but the quantitative verification of the LRM+ procedure remained a challenge.

The achievements made in fabricating and characterizing planar distributed standards in conductive wafer processes observed over the last several years has established a solid background for accurate on-wafer calibration on silicon, e. g. [8-10]. This paper presents a quantitative comparison of the reference multiline TRL[2] [11] and lumped LRM+ [7] for a customized set of standards in a CMOS process using IBM's 0.13 µm technology, with an NFET transistor of gate length 0.12 µm as the DUT. This comparison was undertaken for the first time and covered a frequency range from 1 to 110 GHz.

Additionally, this paper considers proper design of planar structures and presents simulated and measured results of wafer-embedded standards.

Finally, key model parameters of an active DUT are extracted with respect to different wafer-embedded calibration schemes.

II. On-Wafer calibration Comparison

Different calibration procedures have been developed in the past years [12]. All of them rely on ideal, fully or partly known reference elements (calibration standards), realized in planar design (microstrip or coplanar).

In contrast to coaxial and waveguide applications, a great variety of fabrication techniques makes it almost impossible to trace planar calibration standards to a primary reference. This substantially complicates the task of specifying and verifying planar calibrations. However, research undertaken by the National Institute of Standards and Technology (NIST) provided a procedure for comparing wafer-level calibrations,

[1] Line-Reflect-Match, advanced.
[2] Thru-Reflect-Line

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identifying setup drift, as well as verifying calibration standards [13].

In this work, NIST multiline TRL was selected as the benchmark calibration. In conjunction with methods proposed in [14, 15], this procedure allows accurate setting of the measurement system reference impedance to 50 Ohms as well as a precise definition of the measurement reference plane for both semi-insulating and conductive wafers. Thus, it can be successfully applied for verifying the accuracy of a lumped calibration with a wafer-embedded customized set of standards.

III. On-Wafer Calibration Standards

The customized calibration set included all standards required for the benchmark TRL and lumped LRM+ calibrations. The standards were fabricated within a typical 2-port AC GSG on-wafer padset. The ground pads, signal pad, and signal launch lines were placed at a high-level metal layer.

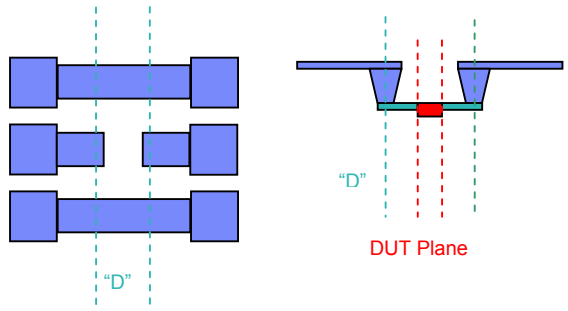

Fig. 1. Design of the customized calibration set.

The transmission lines were fabricated as extensions of the signal launch lines at this high-metal level. Line lengths were optimized to cover a frequency band from 1 GHz to 110 GHz. Lumped load, short, and open elements were developed according to [7] and optimized for the specifics of the bulk CMOS process used and the device under test (DUT) design. These elements were fabricated at the bottom of the via stacks, at plane "D" in Fig. 1, closely coinciding with the placement of the DUT. Thus, both the TRL and LRM+ calibrations establish the reference plane at the via stack, close to the on-wafer DUT.

The electrical parameters of TRL lines were simulated with a simplified model using the 3D full-wave electromagnetic field simulation package Ansoft HFSS®[3]. Simulation of the complete physical structure in Fig. 1 with HFSS requires computing resources and solution times that are not practical, so the structure has to be simplified while retaining the correct response. The simplest approach is a microstrip line, a solid reference conductor, and a single dielectric. This structure was created using the physical dimensions of the launch line, reference plane, and total dielectric thickness.

The cumulative phase of the thru and line standards was used to validate that a single value could be chosen for the real part of the dielectric constant and this would predict the correct phase for all transmission line lengths. The losses of the lines in the model are modulated by the conductivity of the return path and the dielectric loss tangent. These parameters are set in the simplified model to provide a good fit to the measured data.

IV. Measurement Setup

The experimental setup for the 110 GHz wafer-level measurements included an Agilent 8510XF VNA, a semi-automated wafer-probe station, 110 GHz wafer probes with a pitch of 100 μm from GGB Industries, and GaAs reference material RM 8130 available from NIST.

The influence of contact repeatability on measurement data, calibration standards, verification elements, and evaluation transistor S-parameters was reduced by acquiring raw data (with error correction turned off) in three measurement runs. Measurement data from the VNA was recorded with proprietary data acquisition software developed by IBM and with commercial software SussCal®[4]. Off-line LRM+ and TRL calibration, error correction, and calibration comparison was performed using SussCal and MultiCal©[5] software packages.

V. Experimental Results

First, the measurement system drift (instrument drift) shown in Fig. 2 was verified within the time interval of the DUT measurements using the calibration comparison technique and a commercially-available alumina calibration substrate. The probe contact repeatability error is significantly less than the measurement instrument instability within the experimental time (about eight hours) due to fabrication of the standards with gold contact pads. Therefore, it was assumed that the error defined from the calibration comparison method represented the instability of the measurement instrument only.

Also, the contact repeatability error of probing on aluminum pads was found from three identical measurement series A, B, and C, of the same wafer-embedded calibration set. Obtained results showed that the error between series AB, BC and AC are comparable and that it is larger than the instrument drift. It follows that the contact repeatability on aluminum pads

[3] HFSS is commercially-available from ANSYS Inc.

[4] SussCal is available from SUSS MicroTec.

[5] MultiCal software package is available from NIST.

affects experimental results more than the test instrument instability.

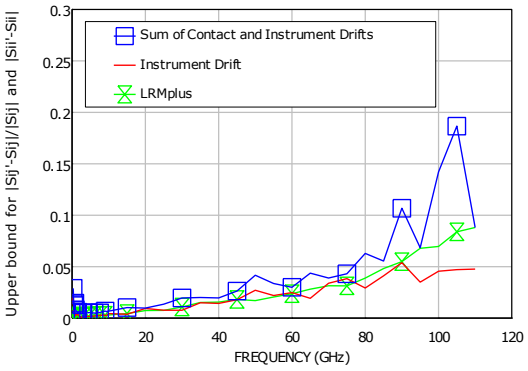

Fig. 2. The accuracy verification of the on-wafer LRM+ calibration.

The line capacitance per unit length was extracted and the characteristic impedance was found using the methods [14, 15]. The extracted value of the line capacitance is 1.5578 pF/cm. The Fig. 3-4 show the measured characteristic impedance, relative phase and attenuation constants of the lines.

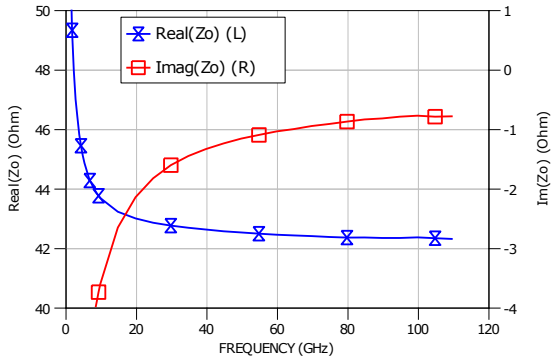

Fig. 3. Measured characteristic impedance of the line standard.

The measured parameters of the customized thru (Fig. 5), load (Fig. 6), and line standards were obtained from the multiline TRL with the reference impedance normalized to 50 Ω. As shown in the figures, the comparison of the measured parameters of standards and the simulation results exhibited good agreement.

Different resistors were compared to evaluate the influence of fabrication tolerances: the load used for the LRM+ calibration and loads from the Open-Resistor, Resistor-Open, Short-Resistor, Resistor-Short structures as illustrated in Fig. 6. All resistor structures had the same layout geometries. It was found that the load impedance variation error was comparable with the contact repeatability error of this experiment.

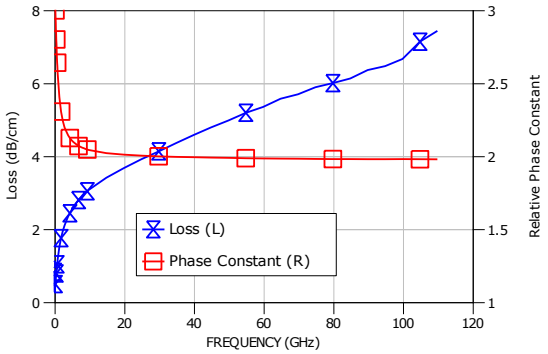

Fig. 4. Measured relative phase and attenuation constants of the line standard.

Next, the on-wafer LRM+ calibration was verified against the benchmark multiline TRL. As shown in Fig. 2, the error of the on-wafer LRM+ is comparable with the system instrument drift and the contact repeatability error for measurements on silicon.

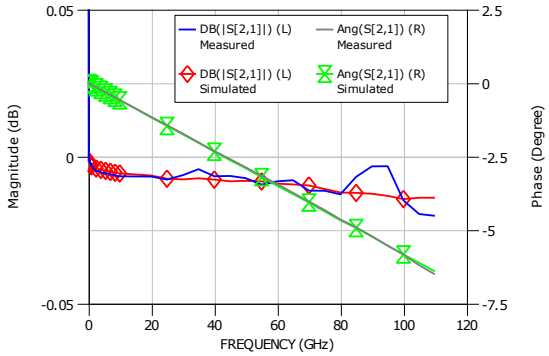

Fig. 5. Comparison of the simulated and measured characteristics of the 24 µm thru standards. The measured parameters were obtained with respect to the multiline TRL calibration method and with the reference impedance normalized to 50 Ω.

Finally, the same NFET transistor with a gate length of 0.12 µm was measured using the conventional two steps probe-tip (off-wafer) SOLT calibration and the open and short DUT contact pads were de-embedded. This data was compared with the data measured using the on-wafer TRL and LRM+ calibration procedures. Key device parameters Cgs and

Cgd were extracted and compared as shown in Fig. 7. These results show both on-wafer calibration methods are comparable and are a significant improvement for critical parameter extraction over the SOLT calibration with open/short de-embedding over the frequency range of 1 to 110 GHz.

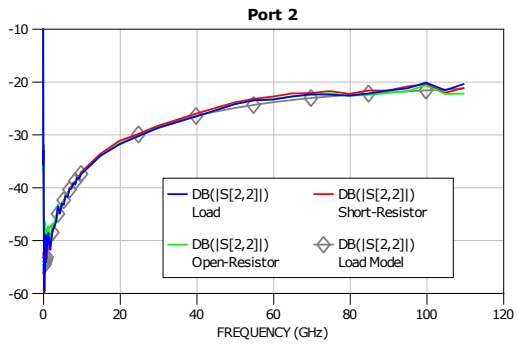

Fig. 6. Comparison of the simulated and measured characteristics of load standard for the second port elements for the LRM+ load, the Open-Resistor, and the Short-Resistor de-embedding structures. The measured parameters were obtained with respect to the multiline TRL calibration method and with the reference impedance normalized to 50 Ω.

VI. Conclusion

Summarizing, for the first time the LRM+ calibration was quantitatively verified on a challenging high performance RF silicon CMOS technology. It was demonstrated that the accuracy of the on-wafer multiline TRL and LRM+ calibration methods outperform the conventional off-wafer calibration with the DUT contact pad parasitics de-embedded.

Both the LRM+ and the benchmark NIST multiline TRL method are in very good agreement. This proves LRM+ to be a valuable tool as it overcomes the main drawback of multiline TRL: construction of wafer-embedded transmission lines. LRM+ does not require long transmission line calibration standards but nevertheless provides comparable calibration accuracy. LRM+, therefore, saves wafer space, minimizing the test chip size to only three standards, realized in the same padset as the DUT. Thus, a fully automated calibration is possible even when using a fixed wafer probe configuration. The required determination of the electrical model of the load standards needed in the calibration can be done easily, e.g., by means of the approaches presented in [7].

As shown above, LRM+ can be successfully used for advanced RF CMOS applications up to 110 GHz.

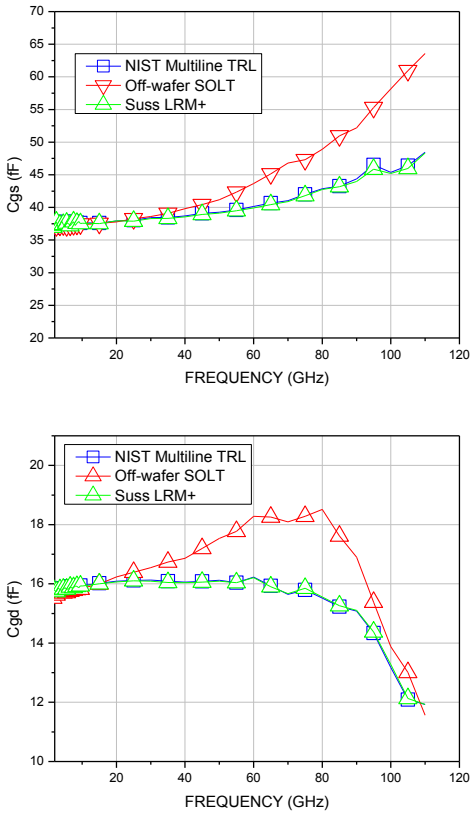

Fig. 7. The test device parameters Cgs and Cgd extracted with respect to the on-wafer multiline TRL and LRM+ calibration procedures and the conventional two-step technique (probe-tip SOLT with the pad de-embedding). The on-wafer TRL and LRM+ shows extremely good agreement over the frequency range and outperforms the conventional method for accuracy of parameter extraction.

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16 ATTACHMENT TO CHAPTER 7

16.1 Paper [64]: “Influence of probe tip calibration on measurement accuracy of small-signal parameters of advanced BiCMOS HBTs”

A. Rumiantsev, P. Sakalas, N. Derrier, and D. Celi, "Influence of probe tip calibration on measurement accuracy of small-signal parameters of advanced BiCMOS HBTs," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Atlanta, GA, 2011.

This paper presented investigation results of the probe-tip calibration impact on the BiCMOS HBT small-signal parameter measurement accuracy. Popular calibration procedures were applied on the same data set and followed by the two-step de-embedding from the device dedicated compete open and complete short dummy elements. This paper proved that only the multiline TRL was capable to establish well-defined calibration reference impedance and to place the measurement reference plane to the desired location. Accuracy of other methods was limited due to imperfection of planar calibration standards and probe misplacement errors. Experimental results showed that the observed difference in cold HBT parameters and parameters of passive devices was minimized by the de-embedding step. The f_T and f_{MAX} demonstrated higher sensitivity to the probe-tip calibration residual errors.

In this work, I developed the methodology of the analysis, planned the work, wrote the major part of the paper and presented the results at a conference. I acquired the measurement data together with Paulius Sakalas University of Technology (TUD) (Dresden, Germany) at the measurement system of the TUD CEDIC laboratory. I did parameter extraction together with Nicolas Derrier and Didier Celi from STMicroelectronics (Crolles, France). The data analysis was shared between all co-authors.

Influence of Probe Tip Calibration on Measurement Accuracy of Small-Signal Parameters of Advanced BiCMOS HBTs

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***Abstract* — This paper presents investigation results of the probe-tip calibration impact on the BiCMOS HBT small-signal parameter measurement accuracy. Popular calibration procedures were applied on the same data set and followed by the two-step de-embedding from the device dedicated Compete-Open and Complete-Short dummy elements. Experimental results showed that the observed difference in cold HBT parameters and parameters of passive devices was minimized by the de-embedding step. The f_T and f_{MAX} demonstrated higher sensitivity to the probe-tip calibration residual errors.**

***Index Terms* — Silicon-germanium HBT, silicon bipolar/BiCMOS process technology, calibration, S-Parameters, de-embedding.**

I. Introduction

Pushing device operation frequencies towards THz range [1] causes serious challenges for conventional device characterization techniques. Presently, RF device characterization uses the two-step approach:

1) probe-tip calibration (off-wafer) that is performed on a commercially available alumina calibration substrate and uses well characterized impedance standards (ISS);
2) de-embedding of the silicon backend parasitics using wafer-embedded test structures such as Open, Short, etc. (also called "dummies").

Each dummy is designed to represent a part (series or parallel) of the backend parasitic impedances. After measurement, these impedances are subtracted by a step-wise procedure yielding characteristics of the device under test (DUT).

A good understanding of possible sources of errors and potential room for improvement of each step are the key factors for increasing the accuracy of device characterization. In this work, we evaluate the impact of popular probe-tip calibration procedures on important Figure of Merits (FoM) and parameters of advanced Si/SiGe:C HBTs from ST Microelectronics' BiCMOS9MW process [2].

Section II describes the calibration procedures that were evaluated, and Section III presents the experimental setup and obtained results for some passive devices as well as for a test HBT under cold and hot (S-parameters) operation conditions. Chapter IV summarizes the observations and gives some practical recommendations for further accuracy improvement.

II. Probe Tip Calibration

For this work, four calibration methods were selected: SOLT[1], LRM+[2], eLRRM[3], and the multiline TRL[4] (or mTRL). These methods have the widest variation from each other in:

1) systematic error models they are built on;
2) types of required calibration standards;
3) definition of calibration reference impedance Z_{REF};
4) sensitivity to standards non-ideality.

A. Calibration Method SOLT

SOLT requires three reflection standards at each VNA measurement port (highly-reflective elements, such as Open and Short, and the well matched 50 Ω Load) and one transmission standard Thru [3]. All electrical characteristics of standards must be fully known. As a result, the calibration accuracy critically depends on the fabrication and characterization of standards. It remains a challenge to achieve reliable SOLT calibration at high frequencies.

B. Self-Calibration Methods: LRM+, LRRM, TRL

The self-calibration methods are based on the seven-term model of systematic measurement errors. They take more measurements of calibration standards than required for calculating error terms. The gained information redundancy enables the use of partly-

[1] Short-Open-Load-Thru
[2] Line-Reflect-Match, advanced
[3] Line-Reflect-Reflect-Match, enhanced
[4] Thru-Reflect-Line

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defined standards. The missing parameters are calculated from within the calibration procedure (also called "self-calibration").

LRM+ uses one transmission (Thru) and two reflection elements: the Load, also called "Match", and the "Reflect" (Open or Short) [3]. The reflection coefficient of the Reflect is a free parameter. This is an important advantage: there is no more need for a well-defined highly reflective element. So far, this has been a challenging task, especially at high frequencies.

Any arbitrary impedance element can be used as the Load. The LRM+ method is capable to set the reference impedance Z_{REF} to 50 Ω when the impedance of the Load standard Z_{LOAD} is known [4].

In contrast to the LRM+, eLRRM uses an additional Reflect avoiding the need for the second port Load [3]. The automatic Load inductance extraction minimizes the calibration error caused by possible probe misplacement on the Load. This algorithm demonstrated reliable results for the well-defined probe-tip calibration conditions (e.g. on alumina ISS).

The multiline TRL was developed at NIST to solve the frequency limitation of the conventional TRL procedure [5]. Operating with many lines, it applies an extensive statistical analysis of the redundant information. In conjunction with the method proposed in [6], this procedure allows precise setting of the calibration reference impedance Z_{REF} to 50 Ω.

Multiline TRL relies on the measurement of sections of transmission lines and does not require any definition of the impedance of the Reflect. Therefore, it became the accuracy benchmark for comparing wafer-level calibrations.

III. Experimental Results

The experimental measurements were carried out on a broadband S-parameter measurement system from Cascade Microtech, consisting of a PM8 manual probe station, 100 micron pitch Infinity probes model SP-i110-A-GSG-03, ISS 104-783A calibration substrate, equipped with the 110 GHz PNA network analyzer from Agilent Technologies. Also, we used the ceramic chuck add-on that carried the ISS and the test wafer to suppress a possible influence of higher order propagation modes and to reduce coupling effects especially at high measurement frequencies [7].

The calibration and error correction were performed for the same data set outside the VNA on a computer. WinCal®[5], MultiCal®[6], and proprietary IC-CAP®[7] script were used for this purpose, while device parameters were extracted using IC-CAP.

It is important to note that due to their size (0.12x14.86 μm^2), the selected test transistors required extremely low input power of about -40 dBm.

The propagation constant γ and the characteristic impedance Z_0 of the ISS lines were extracted using the method from [6]. It resulted in a capacitance per unit length of C=1.481 pF/cm. The reference impedance of the multiline TRL was set back to 50 Ω and the measurement reference plane was moved to the probe tip ends. After that, multiline TRL established well-defined calibration conditions and could be used as the accuracy benchmark.

A. Verification of Passive Elements

The set of dummies included Pad-Open, Pad-Short, and Complete-Open and Complete-Short elements. The Pad-Open and the Pad-Short give the parasitic impedance of the contact pads and can be used in multi-step de-embedding methods or for moving the measurement reference plane to the metal 6 (M6) level (Fig. 1). The pairs of Complete-Open and Complete-Short structures were designed for de-embedding of complete backend parasitics of a specific device geometry and are device optimized.

Raw measurement data of all de-embedding elements were calibrated by the probe-tip SOLT, LRM+, eLRRM and the multiline TRL methods. Assuming the Π-equivalent circuit for the Open and the T-equivalent circuit for the Short dummies, we extracted equivalent capacitances *C1*, *C2* and *C3* and inductances *L1*, *L2*, and *L3* for the Complete-Open and Complete-Short elements respectively (Fig. 2, Table 1). *C3* and *L3* are negligible.

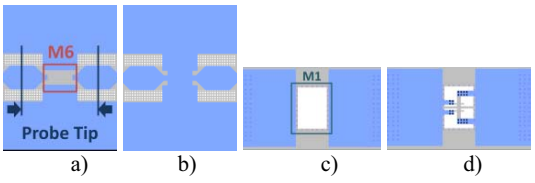

Fig. 1. Pad-Open (a), Pad-Short (b), Complete-Open (c, zoomed), and Complete-Short (d, zoomed) dummies. Location of the measurement plane at the probe tip, M6 (a) and M1 (c).

We observed slight parameter variations that can be attributed to the calibration residual errors. *C1* and *C2* being de-embedded from the Pad Open are about 2 fF. *L1* and *L2* being de-embedded from the Pad Open and the Pad Short are about 7.5 pH for all methods (Fig 2).

[5] WinCal is available from Cascade Microtech
[6] MultiCal is available from NIST
[7] IC-CAP is a product of Agilent Technologies

As de-embedding subtracts impedances, the major part of calibration residual errors vanished.

TABLE I
PARAMETERS OF COMPLETE OPEN AND SHORT

Parameter	Probe Tip Calibration			
	SOLT/ SOLT(m)	mTRL	LRM+/ LRM+(m)	eLRRM
C1, fF	19.7/21.5	21.3	21.6/21.8	21.6
C2, fF	19.6/21.3	22.3	21.4/21.3	22.5
L1, pH	20.1/21.3	24.2	21.7/21.8	21.8
L2, pH	20.5/21.6	24.4	21.9/22.0	22.0

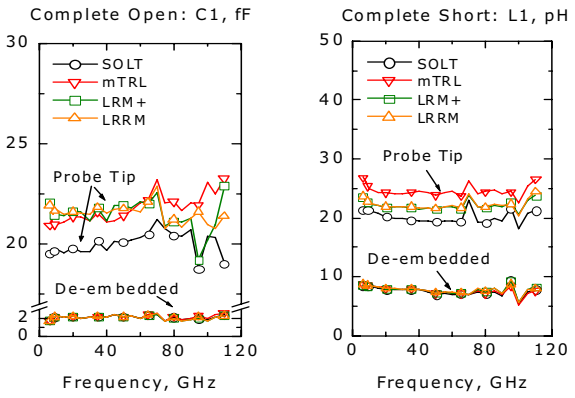

Fig. 2. The capacitance *C1* of the Complete-Open (left) and the inductance *L1* (right) of the Complete-Short elements.

B. Verification for a Transistor

As an active device, we measured S-parameters of a HBT having 14.86 µm length and 0.12 µm emitter stack width at different bias conditions: in a cold-S mode with V_B=-1 V…0.5 V, V_C=0 V and in hot-S (active) mode V_B=0.7 V…1 V and V_{CB}=0 V (emitter grounded in both cases). We extracted some key transistor characteristics: junction capacitances C_{BE} and C_{BC}, f_T and f_{MAX}. f_T was calculated at 20 GHz using the single spot frequency method. The f_{MAX} was defined with Mason's gain. All results were de-embedded from the Complete-Open and Complete-Short dummies. Table II compares obtained parameters.

We found that the probe-tip calibration does not significantly influence de-embedded junction capacitances C_{BE} and C_{BC} up to 67 GHz. f_T is 241 GHz for all methods except SOLT which gave a value lower by 6 GHz. f_{MAX} revealed variations of about 34 GHz in total with the highest value of 329 GHz for SOLT. Obviously, the de-embedding from the Complete-Open and the Complete-Short does not fully compensate for the calibration residual errors in hot-S parameter measurements.

We found that the major portion of the residual errors was caused by the misplacement of probes on calibration standards. SOLT reacts most sensitively, whereas mTRL and eLRRM are significantly less sensitive to probe misplacement [8]. Fig. 4 (left) shows the conductance *G1* of the Pad Open. *G1* is negative for SOLT, which is obviously wrong for any passive element. Such artifacts typically illustrate that the calibration reference impedance was defined incorrectly.

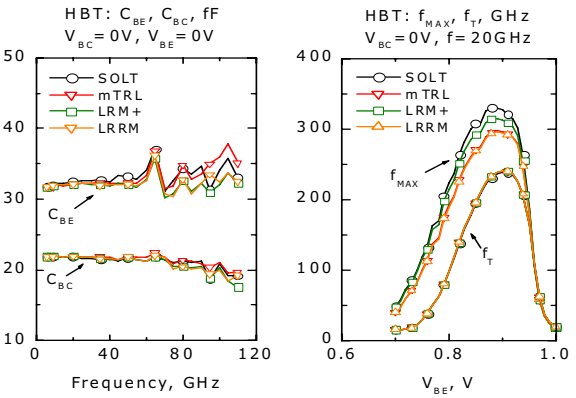

Fig. 3. Extracted junction capacitances C_{BE} and C_{BC} (right), f_T and f_{MAX} of a test HBT (left). Results are de-embedded from the Complete-Open and the Complete-Short dummies.

TABLE II
EXTRACTED PARAMETERS OF TEST TRANSISTOR

Parameter	Probe Tip Calibration			
	SLOT/ SOLT(m)	mTRL	LRM+/ LRM+(m)	eLRRM
C_{BE}, fF[8]	32.2/32.3	32.0	31.9/32.1	32.1
C_{BC}, fF[8]	22.8/22.1	22.8	22.8/22.0	21.9
f_T, GHz [9]	236/242	241	241/241	241
f_{MAX}, GHz[10]	329/302	297	315/298	295

We used the automatic Load inductance extraction algorithm of the eLRRM method to find the actual inductance of the Load [9]. In contrast to the factory value of -3.3 pH, the port 1 *L1* and the port 2 *L2* inductances yielded 0.1 pH and 1 pH respectively (for the frequency range of 20 GHz to 50 GHz). Next, the Open parasitic capacitance and the Short parasitic

[8] V_{BC}=V_{BE}=0V
[9] V_{BC}=0V, V_{BE}=0.9V
[10] V_{BC}=0V, V_{BE}=0.89V

inductance were extracted from the eLRRM-corrected measurements. Then, SOLT was recalculated for the new models of Open, Short and Load. (Fig. 4, legend SOLT(m)). The corrected SOLT(m) was in good agreement with mTRL and eLRRM for both passive and hot-S parameter FoMs (Table 1, Table 2).

Finally, LRM+ was re-calculated for measured *L1* and *L2* of the Load (Table 1, 2, legend LRM+(m)). The variation of f_T and f_{MAX} turned out to be less significant than for SOLT. f_T remained constant, while f_{MAX} decreased by 17 GHz.

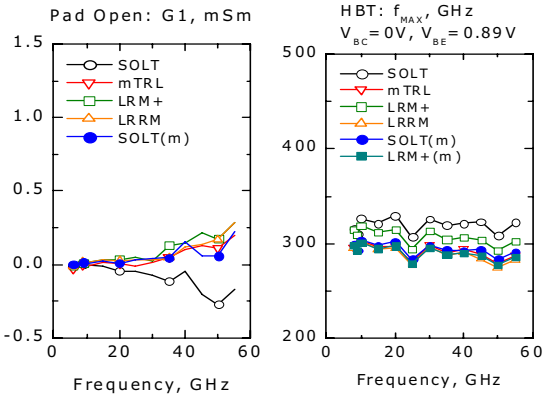

Fig. 4. The conductance *G1* of the Pad Open element (left) and the f_{MAX} of a test transistor (right). The f_{MAX} is de-embedded from the Complete-Open and Complete-Short.

IV. Conclusion

In this work, we investigated the impact of the probe-tip calibration on the measurement accuracy of advanced BiCMOS HBT small-signal parameters. We proved that for frequencies below 67 GHz, the measurement accuracy of the junction capacitances is mainly defined by the de-embedding step, as possible calibration errors (e.g., due to probes misplacement) are cancelled. The required low power of the input signal did not allow drawing a clear conclusion for frequencies above 67 GHz due to the impact of the noise.

We found that the inaccurate probe tip calibration affected f_T and f_{MAX}. Due to the probe misplacement error, SOLT overestimated f_{MAX} by 27 GHz (about 10%) and underestimated f_T by 6 GHz (about 3%). LRM+ demonstrated constant f_T and an overestimation of about 17 GHz (or 5%) for f_{MAX}. Both multiline TRL and eLRRM provided the same results given equal conditions.

The undertaken experiments revealed that the measurement accuracy of the small-signal transistor parameters can be improved by:

1) using advanced calibration methods;
2) reducing the equivalent impedances of the silicon backend parasitics as well as the impact of the probe placement calibration error.

The last can be achieved by the in-situ (on-wafer) calibration step.

Acknowledgement

The EU FP7 IP DOTFIVE project is acknowledged for financial support. Cascade Microtech also acknowledges Agilent Technology EESof division and Dr. Franz Sischka from Agilent for support with IC-CAP. M. Schroter and P. Sakalas are thankful for financial support within the BMBF CoolSilicon project.

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16.2 Paper [59] (Invited Talk): “State-of-the-art and future perspectives in calibration and de-embedding techniques for characterization of advanced SiGe HBTs featuring sub-THz f_T/f_{MAX}"

N. Derrier, A. Rumiantsev, and D. Celi, "State-of-the-art and future perspectives in calibration and de-embedding techniques for characterization of advanced SiGe HBTs featuring sub-THz f_T/f_{MAX}," in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012. IEEE, Portland, OR, 2012, pp. 92-99.

This paper presented an overview of RF calibration and pad de-embedding techniques, discusses limitations and demonstrates methods for accuracy improvement applicable for the characterization of advanced BiCMOS HBTs. The impact of the reference plane location was discussed. Numerous experiments with different device geometries showed that the *in-situ* (on-wafer) calibration yields the most accurate results. For a probe-tip calibration, a multiple-dummy de-embedding is crucial to improve measurement accuracy. A comparison with the compact model (HICUM V2.30) confirmed the findings.

This paper was a joint work with Nicolas Derrier and Didier Celi from STMicroelectronics (Crolles, France). In this work, I planned the paper and the measurement comparison campaign, did all measurements, and performed calibration and de-embedding calculations. I also wrote the related sections of the paper and presented the work at the conference. Nicolas Derrier applied the advanced six-step de-embedding method on the probe-tip calibrated data and provided HICUM compact model verification and created the 3D pictures of standards, de-embedding structures and DUTs. The data analysis was shred between all co-authors.

State-of-the-art and Future Perspectives in Calibration and De-Embedding Techniques for Characterization of Advanced SiGe HBTs featuring sub-THz f_T/f_{MAX}

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***Abstract* — This paper presents an overview of RF calibration and pad de-embedding techniques, discusses limitations and demonstrates methods for accuracy improvement applicable for the characterization of advanced BiCMOS HBTs. The impact of the reference plane location is discussed. Numerous experiments with different device geometries showed that the in-situ (on-wafer) calibration yields the most accurate results. For a probe-tip calibration, a multiple-dummy de-embedding is crucial to improve measurement accuracy. A comparison with the compact model (HICUM V2.30) confirmed the findings.**

***Index Terms* — SiGe HBT, Bipolar modeling and simulation, de-embedding, HF measurements, calibration, S-parameters.**

I. INTRODUCTION

Continuously increasing demand for more content, higher speed and cheaper products pushes development of advanced silicon devices operating near THz range. BiCMOS technologies featuring HBT f_T/f_{MAX} of 220/280 GHz respectively have already become foundry available and address the needs of mass production [1]. Further improvement has recently been achieved for HBTs with 300/500 GHz for f_T/f_{MAX} [2, 3]. Their integration into a 300 mm BiCMOS foundry of 55 nm node is in progress [4].

Though substantial enhancements have already been achieved regarding technology and performance of devices, accurate device characterization and parameter extraction still remain challenging. This originates in the different points of view on the "device" in characterization, modeling, and design engineering communities. Still a subject of debate – the location of the characterization reference plane: at the probe tip, at the lateral device terminals or at one of the levels of the Back End of Line (BEOL). As a result, the following procedure has prevailed as the industry's standard: the RF Figures of Merits (FoM) are extracted at relatively low frequencies (typically at 20 GHz); data are calibrated to the probe tip end by the SOLT method and de-embedded using the OPEN and SHORT contact pad dummy elements [5]. Still, this approach may lead to a serious over/under estimation of FoM of sub-THz f_T/f_{MAX} HBTs [6].

Various investigations were undertaken to improve the accuracy of probe tip calibration and pad de-embedding [7-11]. However, to the authors' best knowledge, a cumulative analysis of calibration and pad de-embedding methods for parameter extraction accuracy across various device geometries is still not available.

This paper presents an overview of RF calibration and pad de-embedding techniques, discusses limitations and demonstrates methods for accuracy improvement applicable for characterization of advanced BiCMOS HBTs. Section II gives a brief summary of the S-parameter calibration background. Section III discusses the optimal location of the measurement reference plane and the proper design of de-embedding elements. It is shown that various transistor geometries may have different requirements. A six-step de-embedding algorithm and the in-situ calibration are proposed as possible solutions to minimize distributive effects in Section IV. Finally, the results of an extensive Design Of Experiment (DOE) are presented in Section V. The DOE was carried out on diverse HBT geometries of ST B5T process transistors and for a wide range of calibration algorithms and de-embedding methods.

II. S-PARAMETER CALIBRATION BACKGROUND

For S-parameter measurements, the systematic measurement errors are represented using the system error model. The purpose of the calibration is to define individual components of this model, the "error terms", and to exclude measurement errors from the DUT data by the error-correction step. Modern VNAs enable application of advanced error models and calibration methods, offering a variety of benefits for measurements at mm-wave frequencies and beyond [12].

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A. Calibration Method SOLT

SOLT[1] requires three reflection and one transmission measurement conditions: Short, Open, Load, and Thru, respectively. All electrical characteristics of standards must be fully known. Subsequently, calibration accuracy critically depends on the design, fabrication and characterization of standards. Though SOLT is one of the widely used algorithms, it remains a challenge to achieve reliable calibration results at high frequencies.

B Self-calibration: Multiline TRL, LRM+, and LRRM

A number of methods use information redundancy to relax requirements to one (or more) standards. Unknown characteristics are subsequently calculated within the calibration process (e.g. "self-calibration").

The multiline TRL[2] (mTRL) was developed at NIST in the early 1990s [13]. It applies advanced statistical analysis of the redundant information gained from measurements of multiple sections of transmission lines of known length. Furthermore, any symmetrical (S_{11}=S_{22}) highly-reflective element can be used as a Reflect. It is sufficient to estimate the phase of its return loss roughly within ± 90 degrees. This is an important advantage for wafer-level application: so far, realizing an ideal or fully-known broadband Open or Short standard has been a challenging task.

Moreover, in conjunction with the method proposed in [14], mTRL calibration reference impedance Z_{REF} can be accurately set to the required value of 50 Ω. Thus, mTRL became the reference method for wafer-level calibration, calibration comparison and accuracy verification.

LRM+[3] uses one transmission (Thru) and two reflection elements: the Reflect (similar to mTRL) and the Load (or "Match"). Any arbitrary impedance element can be used as the Load. The LRM+ method is capable to set the calibration reference impedance Z_{REF} to 50 Ω when the impedance of the Load standard Z_{LOAD} is known [15]. For LRM+, standards can be designed for a constant probe-to-probe distance, significantly reducing the test chip size and enabling an automated calibration.

The enhanced LRRM[4] (or eLRRM) was developed to address the need for accurate broadband probe-tip calibration [16]. The automatic Load inductance extraction embedded in eLRRM minimizes the calibration error caused by probe misplacement on the Load. This algorithm demonstrated reliable results on alumina Impedance Standard Substrate (ISS).

[1] Short-Open-Load-Thru
[2] Thru-Reflect-Line
[3] Line-Reflect-Match, advanced
[4] Line-Reflect-Reflect-Match

III. LOCATION OF THE REFERENCE PLANE

The S-parameter reference plane can be located at:
1) The probe tip end.
2) The top metal level, metal6 (M6), and
3) The transistor terminals, metal1 (M1, Fig. 1).

Contact pad de-embedding moves the reference plane from the probe tip towards the lateral Device under Test (DUT). Advantages and drawbacks of M6 and M1 are repeatedly discussed between design and modeling communities.

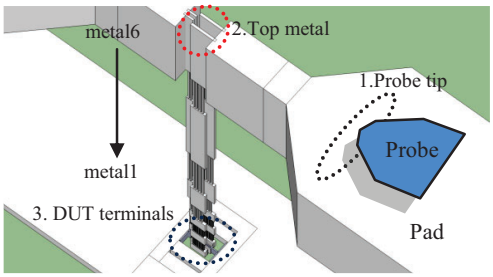

Fig. 1. Three different locations of the reference plane: probe tip, top metal, DUT terminals for a complete-OPEN dummy. Example for the CBEBC HBT, Emitter length of L_E=5 μm.

Design engineers prefer SPICE models that include a minimum of BEOL parasitics and allow realistic pre-layout simulations (schematic mode). Advanced transistors showing very high f_T/f_{MAX}, have junction capacitances of merely several fF. Here, any small parasitics may strongly affect transistor's FoM. Therefore, the top-metal location (e.g. M6) is preferred. For designers, it becomes important that the Process Design Kit (PDK) includes such SPICE libraries.

In contrast, modeling engineers aim to extract "physics-based" parameters of the device compact models. Therefore, the reference plane has to be shifted as close as possible to the intrinsic device terminals (e.g. M1). This paper is mainly focused on device modeling requirements, as they are more challenging.

A. Probe Tip Calibration on ISS

The ISS is an alumina substrate that utilizes several groups of coplanar waveguide elements (CPW): Open, Short, Load, Thru standards as well as transmission Lines of multiple lengths. The equivalent impedances of the Open, Short and Load are represented over a parallel capacitance, serial inductor and a serial connection of an inductor and a resistor respectively. The nominal values depend on the type of ISS, as well as on design, pitch and configuration of a wafer probe and are specified by the vendor. The length of CPW lines is typically optimized to cover a wide frequency range, e.g. from hundreds of MHz up to 110 GHz and beyond. The

Loads are accurately trimmed to R_{LOAD}=50 Ω with typical accuracy better than 0.3 percent. ISS supports various calibration methods, such as SOLT, LRM+, LRRM, mTRL and others.

Due to impact of fabrication inaccuracies as well as a dispersive nature of the CPW lines, additional procedures are required to measure the characteristic impedance Z_{LINE} and the propagation constant γ of the ISS CPW line for accurate TRL calibration[17].

The ISS lumped-standards are significantly better characterized than the custom elements embedded on the test chip. However, their equivalent impedances are sensitive to the probe placement [18]. Inaccurate probe-to-standard alignment may increase calibration residual errors and lead to errors in DUT parameter extraction. As investigated in [6], both mTRL and eLRRM calibration methods are less sensitive to the probe misplacement and are recommended for the probe-tip calibration.

B. Contact Pads and Interconnects Parasitics

A simple method introduced for high-speed bipolar transistors in 1987 allowed characterization of the pad and interconnect parasitics over "dummy" elements [19]. The two-step de-embedding procedure subtracts parallel and serial parasitic impedances, captured by the OPEN (Fig. 2) and the SHORT (Fig. 3) dummies, from the DUT.

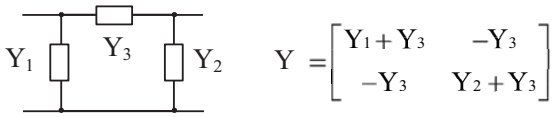

Fig. 2. Π-Equivalent circuit of an OPEN dummy and the Y matrix of parallel parasitics.

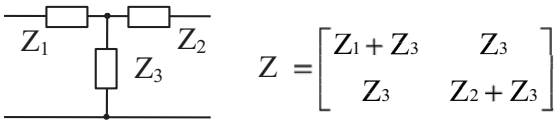

Fig. 3. T-Equivalent circuit of a SHORT dummy and the Z matrix of serial parasitics.

With the increase of the measurement frequency to the mm-wave range, the complexity of the parasitic equivalent circuit increased (e.g. [8, 20]). Furthermore, the distributed effects exhibit stronger impact on de-embedding accuracy. As these effects cannot be captured by the impedance equivalent circuit model, the cascade-matrix based methods and the general four-port de-embedding algorithms were introduced [21, 22]. As a result, the de-embedding process became cumbersome, accumulating a significant area of silicon, and requesting structures which are difficult to be realized (e.g. known Loads). Therefore, such methods are not widely used, making it necessary to develop alternative solutions for accurate measurements at high frequencies.

IV. METHODS FOR ACCURACY IMPROVEMENT

A. The BEOL Parasitics above the Transistor

Previous technologies often used OPEN and SHORT dummies that did not include the via stack and located the reference plane at the top metal (ref. plane n°2, Fig. 1)[5]. Due to the relatively large size of HBTs and the resulting junction capacitances, the coupling capacitances between the emitter, base and collector metal accesses from the top layer down to the first metal layer were negligible.

Advanced mmW technologies made it necessary to review the layout of the OPEN and SHORT dummies: transistor dimensions had shrunk drastically (e.g., the smallest ST B5T HBT has the effective emitter width of W_E=100 nm and the emitter length of L_E=0.520 µm). The BEOL top layers had become thicker reducing transmission line losses. For modeling purposes, it became crucial to shift the de-embedding reference plane down to the first metal layer.

i. The complete-OPEN

To move the reference plane to the DUT terminals, the dummy elements must repeat the geometry of each transistor[6]. The complete-OPEN is a copy of the associated DUT. While excluding the contact vias, it includes all metals and the via stack between the end of the top layer line and the first metal above the DUT (Fig. 1). Fig. 4 shows a magnified view around the first two metals.

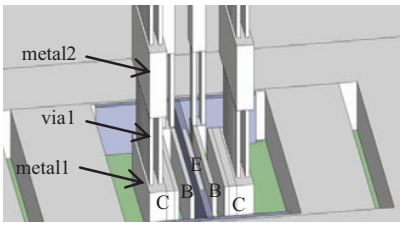

Fig. 4. Magnified view of the area of the M1 and M2 layers of the complete-OPEN. Example for the CBEBC HBT with Emitter length of L_E=5µm.

[5] Such elements will be further called "regular" OPEN and SHORT.
[6] Such elements will be further called "complete" OPEN and SHORT.

Fig. 5 shows f_T de-embedded results (SOLT ISS and OPEN de-embedding) for ST B5T process HBT transistors (section V.*A*) of 2 different lengths (a small one and a medium one). Three different OPEN dummies were used: a regular OPEN (white triangle line, reference plane at top layer M6), a complete-OPEN M1 (black circle line, reference plane at M1, Fig. 4) and a complete-OPEN M2 (white circle line, reference plane at M2). For the small transistor, a difference of 88 GHz on the f_T peak is observed when moving the reference plane from M6 to M1. De-embedding M1 removes additional 1 fF of parasitic capacitance for C_{BE}. The value of the M6-M1 coupling capacitance seems to be small. However, it is in order of the intrinsic capacitance for a small transistor. This ratio reduces with increase of the transistor length.

A prior work attributed the decrease of the f_T for short transistors to the 3D effects [20] whereas it is just a matter of accurate de-embedding and location of the reference plane. Indeed, the f_T FoM should almost be constant for the intrinsic device regardless of its length.

The complete-Open is essential for accurate extraction of FoM for small devices. The obvious drawback is the significant increase of the test chip size.

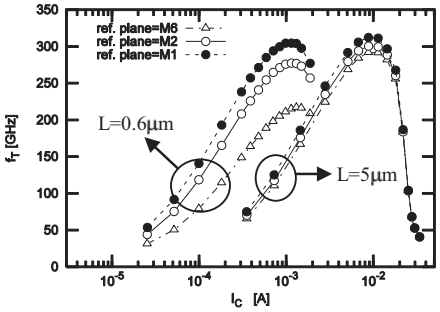

Fig. 5. f_T [GHz] vs collector current [A] (extracted at 20 GHz and V_{CB}=0 V), for two HBT of L_E=0.6 μm and L_E=5 μm, with OPEN de-embedding using three different reference plane locations: Metal6 (white triangle line), Metal2 (white circle line), Metal1 (black circle line).

ii. The complete- SHORT

The complete-SHORT is drawn from the DUT test structure by removing the device and shortening the access to the transistor pins with the M1 plate (Fig. 6).

Similar to the complete-OPEN, the benefit of the complete-SHORT strongly depends on the device geometry. The SHORT de-embedding is more relevant for long or multi-fingers transistors (Fig. 7): due to their small resistances they are very sensitive even to minor series parasitics.

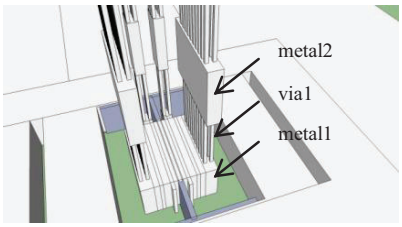

Fig. 6. Magnified area around Metal1 and Metal2 layers of the complete-SHORT.

Fig. 7 clearly demonstrates a resonance around 60 GHz (left plot, circle line) of the inductance parasitics on the C_{BE} RF signature. The right plot shows an improvement of 78 GHz for f_T peak due to accurate de-embedding of the base (Port 1) and the collector (Port 2) resistances by the complete-SHORT.

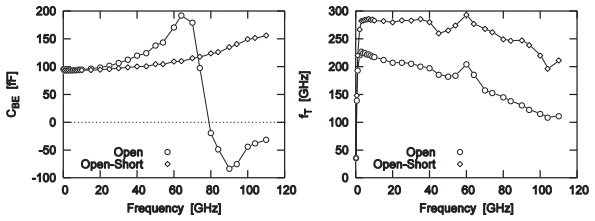

Fig. 7. The Base/Emitter capacitance C_{BE} [fF] @V_{BE}=0 V (left plot) and peak f_T [GHz] (for J_C=15 mA/μm^2) @V_{BC}=0 V (right plot) vs frequency [GHz], for a five Emitter finger HBT of L_E=10 μm after a complete-OPEN (circle) and complete-OPEN/SHORT (diamond) de-embedding.

B. The Importance of the Distributed Effect

Another subject of discussion is the lumped or distributed nature of the de-embedding method. The introduction of the THRU to the OPEN/SHORT sequence did not show a noticeable improvement up to 170 GHz [23].

An advanced de-embedding approach was proposed in [20, 23]. It successively captures the wafer parasitics from the probe tip down to the DUT terminals. Though it implements six steps, all dummy elements are easy to be realized, offering a significant advantage over the four-port method. Extending this methodology with the complete-OPEN and the complete-SHORT, the de-embedding sequence follows as:

1) Probe-SHORT (reduces calibration residuals);
2) Pad-OPEN (parallel impedance of the pad);
3) Pad-SHORT (series impedance of the pad);
4) THRU (distributed parallel impedance of the line);
5) complete-OPEN (parallel impedance of the metal/via access above the transistor);

6) complete-SHORT (series impedance of the metal/via access above the transistor);

The equivalent circuit of this method is shown in Fig. 8.

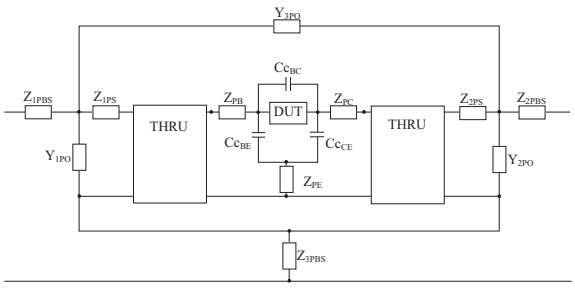

Fig. 8. The equivalent circuit of the 6-dummy de-embedding

Fig. 9 compares the complete OPEN/SHORT (circle lines) against the six-dummy method (diamond lines) for the C_{BE} and f_T FoM. Both are based on the ISS SOLT calibration. The 6-dummy method significantly outperforms above 40 GHz.

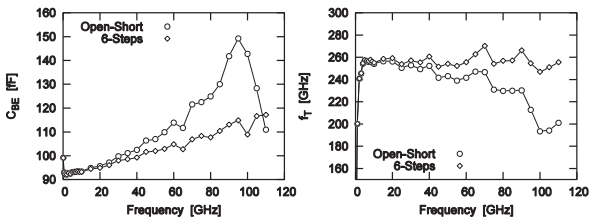

Fig. 9. Base/Emitter capacitance C_{BE} [fF] @V_{BE}=0 V (left plot) and peak f_T [GHz] (for J_C=15 mA/μm^2) @V_{BC}=0 V (right plot) vs. frequency [GHz], for a five Emitter finger transistor L_E=10 μm after the complete-OPEN/SHORT (circle) and the six-steps (diamond) de-embedding.

C. In-situ (On-Wafer) Calibration

Still, the advanced de-embedding method presented above suffers from its complexity [20, 23]: a measurement campaign targeting a scalable library of 30-40 transistors and several temperature conditions will require a tedious and lengthy post-processing of data.

In opposite, the in-situ calibration (with standards implements on a test chip) allows moving the reference plane close to the DUT terminals in one step. The remaining BEOL parasitics are significantly minimized, so that a simple two-step de-embedding method can be used to capture them.

The first in-situ calibration attempts were made in the late 1990s [24]. It was found that the fabrication inaccuracy did not allow implementation of the conventional SOLT procedure on the Si wafer. Over the past years, substantial achievements have been made in fabricating and characterizing planar standards in processes with a conductive substrate (e.g. [10, 25, 26]). LRM+ and mTRL turned out to be the most appropriate methods for in-situ calibration on conductive wafers.

The required calibration elements utilize the same contact pad design as the DUT. The Thru and the Lines are designed as M1-shielded 50 Ω top metal grounded coplanar waveguide. The effective Line length is: 51, 549, 1545, and 3039 μm respectively, covering the frequency range from 1 GHz to 110 GHz. The symmetrical Reflect is a CPW short located at the M1 level. The Load is a single (per port) symmetrical 50 Ω N+ salicided poly resistor located at the M1 level. The calibration reference plane is set at the top metal level.

i. Notes about In-Situ LRM+

The Load element takes a crucial position as it defines the LRM+ calibration reference impedance. The resistance of the in-situ Load is affected by the fabrication variability and may differ from chip to chip. That is why it should be measured during the calibration process. The source monitor unit (SMU), that is used to bias the DUT, provides sufficient accuracy for the measurement of the Load resistance.

The Load reactance is mainly represented by the equivalent reactance of the via stack (the distance between M6 and M1). This parameter can be simulated during the design step as it is less sensitive to the fabrication process instability. Alternatively, it can be measured with respect to the probe-tip calibration and the two-step de-embedding [26].

ii. Notes about In-Situ mTRL

The TRL sets the calibration reference impedance to the Line characteristic impedance Z_0 and the measurement reference position to the center of the Thru. Both the propagation constant γ and the Z_0 of the Line are required to shift the measurement reference plane to an arbitrary position and to transform the calibration results to the 50 Ω system reference impedance. The calibration comparison [27] or the lumped load method [14] can be used to extract the Z_0 of the in-situ lines.

V. EXPERIMENTAL RESULTS

A. The Design Of Experiments (DOE)

The objective of the DOE was to answer the following questions:

1) What is the most suitable calibration method?
2) What is the advantage of in-situ over probe-tip calibration?
3) Which type of de-embedding dummies gives the best results?

STMicroelectronics B5T process featuring f_T/f_{MAX} of 300/400 GHz at collector current density J_C of

15 mA/µm² was used for the experiment [2, 28]. Seven characterization strategies (TABLE I) were applied to the measurement of 4 HBT geometries (TABLE II).

TABLE I
LIST OF CALIBRATION AND DE-EMBEDDING EXPERIMENTS

Experiment	Calibration standards	Calibration algorithm	De-Embedding dummies
n°1	ISS	SOLT	O+S*
n°2	ISS	LRRM	O+S*
n°3	ISS	LRM+	O+S*
n°4	ISS	mTRL	O+S*
n°5	in-situ	LRM+	O+S*
n°6	in-situ	mTRL	O+S*
n°7	ISS	SOLT	6-dummies

* complete Open + complete Short

TABLE II
LIST OF MEASURED TRANSISTORS

Process	Geometry	Emitter width*, µm	Emitter length, µm
ST B5T	CBEBC	0.18	0.6
	CBEBC	0.18	5
	CBEBC	0.18	15
	C-5x(BEBC)	0.18	10

* drawn dimensions

B. The Measurement Setup

The experiment was carried out on a broadband S-parameter measurement system from Cascade Microtech, consisting of a semi-automated wafer-probe system Elite300™-AP, a pair of 110 GHz GSG Infinity Probes® of 100 µm pitch and a fitting alumina calibration[7] substrate (ISS), equipped with broadband 110 GHz PNA-X VNA and 4142B SMU from Agilent Technologies. The DUT input and output power level (port 1 and port 2) was set to -35 dBm and -15 dBm to protect the DUT from overload.

The measured data of the ISS and in-situ standards, the de-embedding structures and the test transistors were acquired in raw format (with the S-parameter calibration turned off). The calibration and error correction were performed by WinCal XE™, and proprietary IC-CAP script outside of the VNA on a computer and for the same raw data set. This approach ensured a minimal impact of contact repeatability and instrument drift on the accuracy of experimental results. Device parameters were extracted using IC-CAP.

C. Results on the Transistors

i. Cold [S] Parameter Results

Fig. 10 shows the Base/Collector capacitance for long multi-fingers transistors extracted from cold [S] measurements. Only the in-situ calibration (both LRM+ and mTRL) gives the expected RF signature of the π-equivalent circuit, which corresponds to the DUT in cold-[S] mode (0 V bias): the capacitances remain constant up to 110 GHz. The in-situ calibrations outperform probe-tip methods from 40 GHz for multi-finger and from 70 GHz for small transistors.

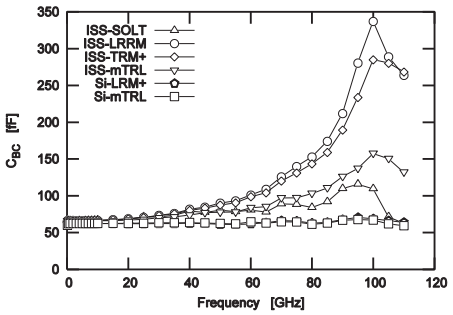

Fig. 10. Base/Collector capacitance C_{BC} [fF] vs frequency [GHz] @V_{BC}=0 V, for a five Emitter finger HBT of L_E=10 µm.

ii. Forward mode [S] Parameter Results

Figure 11 shows peak f_T FoM for a multi-fingers device. Again, only the in-situ calibration methods (LRM+ or mTRL) give expected results for constant f_T up to 110 GHz. For [Y]-parameters in forward mode, the comparison leaded to the same conclusion (not shown here).

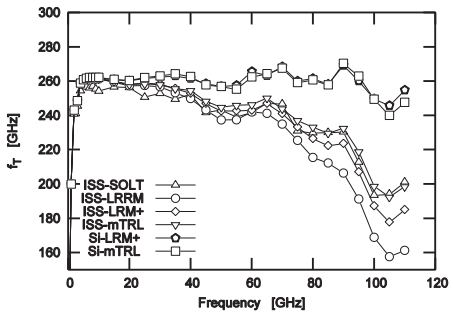

Fig. 11. Peak f_T [GHz] (for J_C=15 mA/µm²) vs. frequency [GHz] @V_{BC}=0 V, for a five Emitter finger HBT of L_E= 10 µm.

D. Probe Tip Calibration and Six-Dummy De-Embedding vs. in-situ Calibration and Open/Short De-embedding

Results presented in section V.*C* are based on the two-step de-embedding method, which is widely accepted as industry standard (TABLE I), [5, 19]. As proved above, a simple two-steps de-embedding yields sufficient results for the in-situ calibration.

As explained in IV.B, the six-dummies de-embedding equivalent circuit accurately captures parasitics remaining after the probe-tip calibration. Consequently,

[7] IC-CAP is a product of Agilent Technologies, Inc.

the next experiment explored in how far this method improves the accuracy of the probe-tip calibration.

Fig. 12 compares the f_T FoMs for the probe-tip SOLT followed by the Open/Short de-embedding versus the six-dummies de-embedding, as well as for the in-situ LRM+ and the in-situ mTRL+, both followed by the Open/Short de-embedding. The implementation of the six-steps de-embedding for the probe-tip calibration yielded results comparable to the in-situ methods for the investigated frequency range. [Y]-parameters showed up the same trend (not shown here).

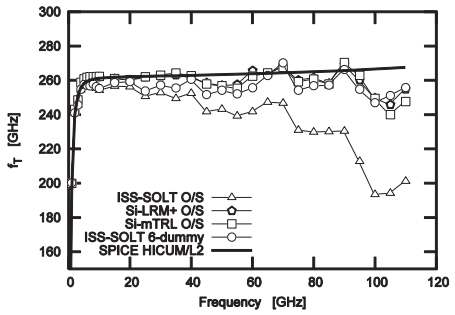

Fig. 12. Peak f_T (for J_C=15 mA/μm^2) [GHz] vs. frequency [GHz] @V_{BC}=0 V, for a five emitter finger HBT of L_E=10 μm, after the SOLT probe-tip calibration + complete-OPEN/SHORT (white triangle) versus six-dummies de-embedding (white circle), in-situ calibrations (white diamond and square), and the HICUM V2.30 compact model simulated with ADS software (solid line).

E. Comparison with a Compact Model

Parameters of the compact model HICUM Level2 (L2) v2.30 [29, 30], for transistors described in TABLE II, were extracted from DC and [S] measurements data, calibrated by the probe-tip SOLT and Open/Short de-embedded. RF FoM like f_T or f_{MAX} were computed at 20 GHz and used inside the extraction sequence, in order to avoid parasitic effects. ADS[8] 2011.10 software was used to simulate the obtained model cards, and compare the simulation with the different calibration/deembedding strategies. Fig. 12 shows that the in-situ calibration and the advanced six-dummies de-embedding validate the model for the entire frequency range of the experiment. The [Y]-parameters demonstrated the same trend (not shown here). Because the HICUM compact model is based on the device's physics, this comparison is an alternative proof of the quality of in-situ methods and the multiple-dummies de-embedding.

[8] ADS is a product of Agilent Technologies, Inc.

VI. CONCLUSION

This work investigated the impact of common calibration methods, de-embedding sequences, and design of de-embedding dummies on the accuracy of S-parameter measurement and FoM extraction of advanced BiCMOS HBTs, featuring f_T/f_{MAX} of 300/400 GHz. It was shown that it is crucial to locate the reference plane close to the device terminals yielding an increase of up to 30 percent of f_T/f_{MAX} for small transistors. For these elements, the M6-M1 coupling capacitance is in order of the intrinsic capacitance for a transistor. It can be completely removed by the introduced complete-OPEN/SHORT dummy elements.

Because the impact of the distributed parasitic effects increases with frequency, a simple two-steps de-embedding failed above 40 GHz for long or multi-finger devices. That is why, an advanced de-embedding, such as the six-steps method, is crucial for measurement accuracy improvement for the probe-tip calibration. The choice of the advanced calibration methods (e.g. mTRL and eLRRM) was not decisive.

The numerous experiments on several ST B5T HBT geometries revealed a substantial accuracy improvement when using the in-situ calibration (mTRL or LRM+). The in-situ standards are optimized to calibrate out the major part of the backend parasitics and to move the measurement reference plane to the M6 level in one step. The remaining M6-M1 parasitics can be removed by a simple two-steps de-embedding. A comparison with the compact model (HICUM V2.30) confirmed the findings.

Though both methods (the probe-tip calibration with six-steps de-embedding and the in-situ calibration with two-steps de-embedding) yield close results, in practice, the choice of the method depends on the available technology and individual preferences.

The in-situ calibration requires preparation work to characterize several electrical parameters of standards. In return, a simple two-step de-embedding can be applied.

The probe-tip calibration demands for an advanced six-steps de-embedding with dummies easy to be realized. However, its application is cumbersome and demands additional silicon area.

ACKNOWLEDGEMENT

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particular Dr. Franz Sischka for support with IC-CAP and valuable discussions.

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17 ATTACHMENT TO CHAPTER 8

17.1 Paper [88]: “Verification of wafer-level calibration accuracy at cryogenic temperatures”

A. Rumiantsev, R. Doerner, and P. Sakalas, "Verification of wafer-level calibration accuracy at cryogenic temperatures," in *ARFTG Microwave Measurements Conference-Fall, 68th,* 2006, pp. 134-140.

This article presented the results of accuracy verification of wafer-level calibration at cryogenic temperatures based on coplanar calibration standards. For the first time, the electrical characteristics of commercially available coplanar calibration lines were extracted at the temperature of liquid helium. It was demonstrated that the temperature dependent variation of the characteristic impedance of the tested lines is within ±1% tolerance of the nominal value of 50 Ω for a temperature range from room temperature down to 4 K. Finally, the accuracy of the transfer TMR calibration method at cryogenic temperatures was verified by definition of the worst case error bounds for the measurement of passive devices and compared to the reference NIST multiline TRL.

It was a collaborative work with Ralf Doerner from Ferdinand-Braun-Institut (FBH), Leibniz-Institut fuer Hoechstfrequenztechnik (Berlin, Germany) and Paulius Sakalas from Dresden University of Technology (TUD) (Dresden, Germany). My contribution to this work was the idea, planning of the work, development of the test and verification methodology, data acquisition, some calculations and data analysis, as well as writing the paper. Ralf Doerner contributed to the calculation and data analysis of this work while Paulis Sakalas assisted the measurement session.

Verification of Wafer-Level Calibration Accuracy at Cryogenic Temperatures

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***Abstract* — This article presents the results of accuracy verification of wafer level calibration at cryogenic temperatures based on coplanar calibration standards. For the first time, the electrical characteristics of commercially available coplanar calibration lines were extracted at the temperature of liquid helium. It was demonstrated that the temperature dependent variation of the characteristic impedance of the tested lines is within ±1% tolerance of the nominal value of 50 Ω for a temperature range from room temperature down to 4 K. Finally, the accuracy of the LRM+ calibration method at cryogenic temperatures was verified by definition of the worst case error bounds for the measurement of passive devices and compared to the reference NIST multiline TRL.**

***Index Terms* — cryogenic, calibration, error correction, calibration comparison, scattering parameters measurement.**

I. Introduction

Accurate calibration is crucial for device measurement, characterization and modeling. Fabrication uncertainty, temperature instability, and mismatch in modeling of calibration standards significantly reduce the final calibration accuracy. Difficulties in traceability of wafer level (planar) calibration standards challenge alternative methods of their verification [1]. These difficulties increase if standards operate in extreme conditions like high vacuum and at the temperature of liquid helium.

The research undertaken by the National Institute of Standards and Technology (NIST) provides a technique for characterizing coplanar lines [2, 3], accurate system calibration [4] and accuracy verification of different calibration methods [5]. This technique is well-accepted in engineering practice and can be successfully used for calibration verification purposes [6]. However, traceable verification results can be achieved only at room temperature and using the reference material RM 8130: the NIST fabricated and characterized GaAs calibration elements [7].

Previously published results of calibration at low temperatures do not consider the temperature influence on the electrical characteristics of thru and line standards [8–11]. Investigations were primarily focused on the temperature stability of thin-film resistors (used as the load standard) as well as on comparing different calibration methods. However, as it was recently demonstrated in [1], even small variations of the electrical parameters of thru and line standards can lead to significant calibration and finally measurement errors. This paper will present the results of extracting electrical characteristics (capacitance per unit length, characteristic impedance Z_0, attenuation and relative phase constants) of commercially available alumina coplanar lines at temperatures down to 4 K, temperature stability of the thin-film load resistance, and finally the accuracy of the LRM+ calibration method at these temperatures.

Fig. 1. The PMC200 cryogenic measurement system used for experiments.

II. Verification Method

The calibration comparison technique [5] was used for the evaluation of time and temperature drift of the cryogenic wafer-level RF measurement system during the experiment and for the verification of the LRM+ calibration method. This

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technique provides the worst-case deviations of the measured S-parameters of passive devices for an examined (first-tier) calibration with respect to a benchmark (second-tier) calibration. Deviations are treated as $|S_{ij} - S_{ij}'|$, for $ij \in \{11, 12, 21, 22\}$, where S_{ij}' is the S-parameter measured by the calibration to be tested, and S_{ij} is the S-parameter measured by the benchmark calibration.

The system drift can be quantitatively defined using the same calibration method with measurements of identical standards once, as the examined calibration, at the beginning of the experiment and again, as the benchmark calibration, at the end. In the ideal case, both calibrations, examined and benchmark, are equal and the error bounds $|S_{ij} - S_{ij}'|$ are zero. Remaining differences can be addressed mainly to system drift and contact repeatability.

Using the calibration comparison technique for the verification of the LRM+ calibration method requires a benchmark calibration. The multiline TRL [1, 4] is well-suited for this purpose and enables an accurate setting of reference plane and reference impedance if the parameters of the line standards are known.

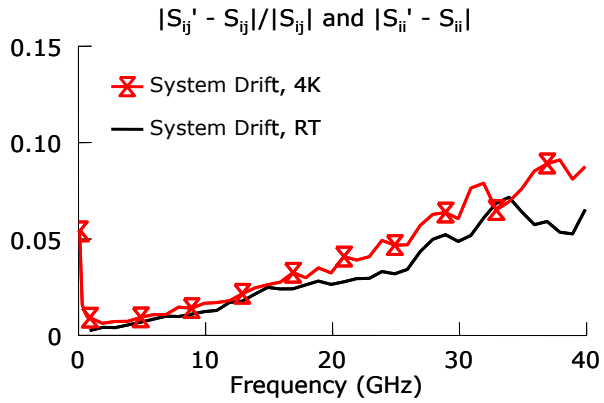

Fig. 2. The system drift of the experimental setup at different temperatures.

To characterize calibration lines at different temperatures the procedure proposed in [2] and evaluated in [1] was used. The resistance R of the load standard can be measured using the 4-terminal method. Then, a first-tier multiline TRL can be performed setting the calibration reference impedance to the characteristic impedance Z_0 of the alumina lines used. The propagation constant known from multiline TRL can be used to extract the value of the line capacitance per unit length C in the frequency range where the tested lines are no longer dispersive and the load reactance is negligible [2, 3]. Once the line capacitance per unit length is found, the characteristic impedance can be obtained from the propagation constants with the help of the MultiCal®[1] software package. The exact determination of the load is essential for accurate line parameter extraction.

[1] Available from NIST, USA

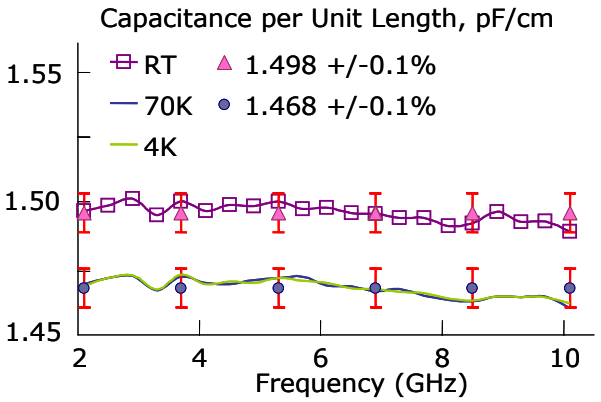

Fig. 3. The results of the line capacitance extraction for different temperatures: room temperature (RT), 70 K, and 4 K. The mean values of 1.498 pF/cm for room temperature and 1.468 pF/cm for 70 K and 4 K data are calculated with maximum error bounds of ±0.1%.

III. Experimental Setup

The experimental setup (Fig. 1) included a high-frequency, manual cryogenic probe system PMC200, 40 GHz GSG |Z| Probes with 150 µm pitch, CSR-8 calibration substrate, SussCal® calibration software (all available from SUSS MicroTec), the Agilent 8722ES opt. 400 40 GHz vector network analyzer (VNA) and the NIST MultiCal® software package. To avoid additional uncertainty due to contact repeatability, all required data were acquired in one measurement series in raw-data format with the help of the calibration software SussCal® and saved externally for further analysis.

Three measurement experiments were performed: one each at room temperature, 70 K and 4 K. The system drift was defined for two extremely different conditions: experiments performed at room temperature and at 4 K and over a time period of 3.5 hours and 4 hours respectively (Fig. 2).

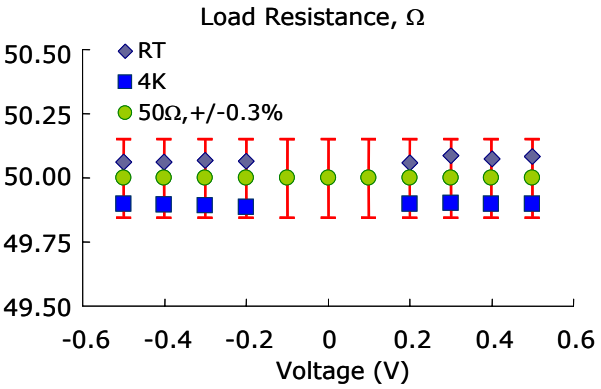

Fig. 4. Load resistance measured over applied voltage of -0.6…+0.6 V at room temperature (RT) and 4 K. The values within -0.1…+0.1 V does not provide acceptable measurement accuracy and are not shown in the graph.

It was found that, considering the 30-minutes difference in experiment time, the drift at 4 K is comparable with the drift at room temperature. It proves that the test system reached a stable condition and validates the measurement data acquired at cryogenic temperatures.

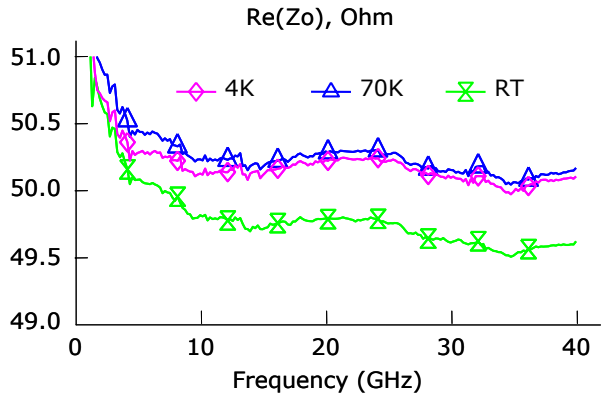

Fig. 5. The extraction results of the line characteristic impedance for the CSR-8 substrate at different temperatures. The extracted values are within the error bounds of ±1% over the range from room temperature down to 4 K.

IV. Results

The line capacitance of the tested CSR-8 alumina substrate was extracted at room temperature, 70 K and 4 K (Fig. 3). To guarantee accurate extraction results, the load resistance was measured at required temperatures. Fig. 4 shows the value of the load resistance provided by the four-terminal method and used for definition of the CSR-8 line capacitance per unit length. The capacitance values are: 1.498 pF/cm at room temperature and 1.468 pF/cm at 70 K and 4 K with maximum error bounds of ±0.1%. The line capacitance per unit length was also extracted at 70 K. No significant difference was observed between the results at 4 K and 70 K.

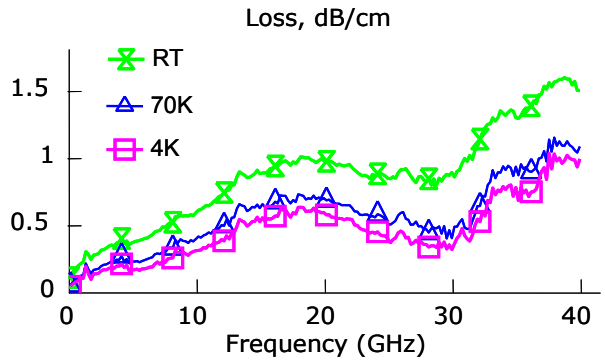

Fig. 6. The extraction results of the attenuation constant at different temperatures.

Next, the characteristic impedance (Fig. 5) was obtained from the measured propagation constant (Fig. 6 and 7). The temperature stability of the characteristic impedance is within ±1% over the range from room temperature down to 4 K. Additionally, the room temperature results demonstrate very good agreement with those extracted using a different setup [1].

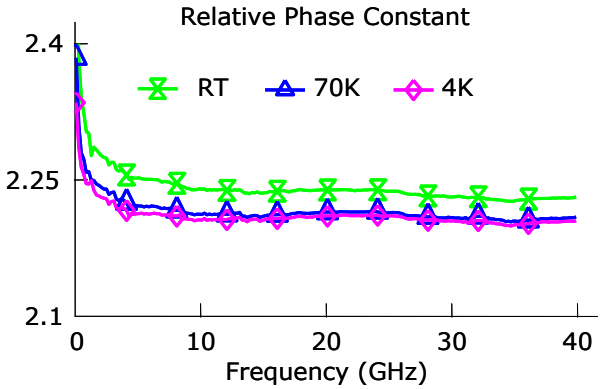

Fig. 7. The extraction results of the relative phase constant at different temperatures.

The temperature dependence of line attenuation and relative phase constants demonstrated expected behavior: decreasing loss and electrical lengths with decreasing temperature. If these effects are not considered when calibrating at different temperatures, they decrease calibration and, finally, measurement accuracy.

Finally, the accuracy of the lumped LRM+ calibration was examined and compared to the multiline TRL in different conditions: at room temperature and 4 K as well as with a full and simplified description of the thru standard. The full description considered the extracted characteristic impedance and propagation constant of the thru standard. The simplified description assumed that the thru standard was lossless, its characteristic impedance was 50 Ω, and the electrical length was known (e.g. 1.16 ps for the used CSR-8 calibration substrate).

Fig. 8 and 9 demonstrate the verification results of the LRM+ calibration with full and simplified characterization of the thru standard at RT and 4 K. The error due to the simplified thru description is negligible for 4 K and slightly decreases calibration accuracy at room temperature from approximately 35 GHz. This effect can be explained by the fact that the LRM+ calibration defines the system reference impedance from the impedance of the load standard. As demonstrated, the electrical characteristics of the used thin-film load element remain stable and ensure the quality of the cryogenic LRM+ calibration over the whole temperature range of interest.

The mismatch between the simplified model of the thru standard and its real characteristics can lead to the error in definition of the measurement reference plane. According to the experimental results, this error is marginal at cryogenic temperatures and at room temperature up to 40 GHz. Therefore, the simple model of the CSR-8 thru standard can

be used at low-temperature calibration and will not lead to significant calibration error.

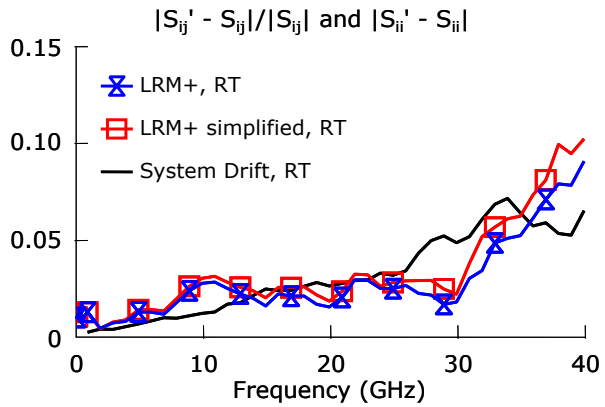

Fig. 8. Verification of the LRM+ calibration method at room temperature using a full and simplified thru description.

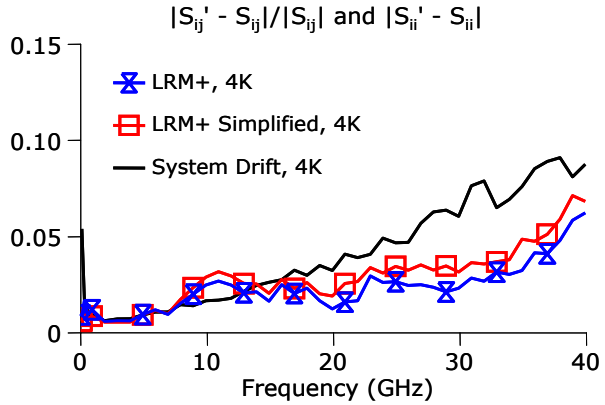

Fig. 9. Verification of the LRM+ calibration method at 4K using a full and simplified thru description.

V. Conclusion

Summarizing, the proven worst-case deviations of the measured S-parameters of passive devices at the temperature of 4 K for the examined LRM+ calibration with respect to the benchmark NIST multiline TRL are less than 0.1 up to 40 GHz and they are less then the measurement system drift within the experiment time. Therefore, the LRM+ method provides calibration accuracy comparable to the NIST reference multiline TRL for the extremely wide temperature range: from room temperature down to 4 K.

The demonstrated temperature stability of the thin-film resistor of the CSR-8 load standard is ±0.3% for the evaluated temperature range. The full characterization of the CSR-8 thru standard is not necessary at low-temperatures. Therefore no additional efforts in characterizing calibration standards are required for accurate LRM+ calibration of a cryogenic wafer-level measurement system.

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17.2 Paper [89]: “Verification of wafer-level calibration accuracy at high temperatures"

A. Rumiantsev and R. Doerner, "Verification of wafer-level calibration accuracy at high temperatures," in *ARFTG Microwave Measurements Conference-Spring, 71st,* 2008, pp. 103-106.

This article presented the results of accuracy verification of wafer-level calibration at high temperatures based on coplanar calibration standards. The electrical characteristics of different commercially available coplanar calibration lines were extracted and compared at different temperatures. Finally, the accuracy of lumped calibrations at variable temperatures was verified by definition of the worst-case error bounds for the measurement of passive devices and compared to the reference NIST multiline TRL.

For this work, I developed the idea, the test and the verification methodology, planned the work, and wrote and presented the paper. Ralf Doerner from Ferdinand-Braun-Institut (FBH), Leibniz-Institut fuer Hoechstfrequenztechnik (Berlin, Germany) did all experimental measurements at the FBH facility. The calculation and the data analysis were shared.

This paper received the Best Interactive Forum Paper Award of the ARFTG-71st Spring Conference.

Verification of Wafer-Level Calibration Accuracy at High Temperatures

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***Abstract* — This article presents the results of accuracy verification of wafer-level calibration at high temperatures based on coplanar calibration standards. The electrical characteristics of different commercially available coplanar calibration lines were extracted and compared at different temperatures. Finally, the accuracy of lumped calibrations at variable temperatures was verified by definition of the worst-case error bounds for the measurement of passive devices and compared to the reference NIST multiline TRL.**

***Index Terms* — calibration, error correction, calibration comparison, scattering parameters measurement.**

I. Introduction

Accurate calibration is crucial for device measurement, characterization and modeling. Fabrication uncertainty, temperature instability, and mismatch in modeling of calibration standards significantly reduce the final calibration accuracy. Difficulties in the traceability of wafer-level (planar) calibration standards challenge alternative methods of their verification [1, 2]. These challenges increase if standards operate in extreme conditions such as very low or high temperatures.

Previous research (i.e. [3, 4]) has already addressed the subject of high-temperature calibration. Investigations focused on the temperature stability of the thin-film resistors (used as the load calibration standard) [3] or on the compensation for the temperature drift of the measurement system [4]. The temperature influence on the electrical characteristics of calibration thru and line standards was, however, not considered. Recently, as demonstrated in [1], even small variations of the electrical parameters of thru and line standards can lead to significant calibration and thus measurement errors.

II. Verification method

The research undertaken by the National Institute of Standards and Technology (NIST) provided a technique for characterizing coplanar lines [5], [6] accurate system calibration [7] and accuracy verification of different calibration methods [8]. This technique is well accepted in the engineering practice and can be successfully used for calibration verification purposes [9, 10]. On the other hand, traceable verification results can be achieved only at room temperature and using the reference material RM8130: the NIST-fabricated and characterized GaAs calibration elements.

This paper demonstrates the results when extracting electrical characteristics (attenuation and relative phase constants) of commercially available alumina coplanar lines and the accuracy verification of different calibration procedures at temperatures up to 150ºC using the method reported in [6].

To define the time and temperature drift of the high-temperature wafer-level RF measurement system during the experiment, the calibration comparison technique was used [8]. This technique provides the worst-case deviations of the measured S-parameters of passive devices for the examined (first-tier) calibration with respect to the benchmark (second-tier) calibration. Deviations are treated as $|S_{ij}-S_{ij}'|$, for $ij \in \{11, 12, 21, 22\}$, where S_{ij}' is the S-parameter measured by the calibration to be tested, and S_{ij} is the S-parameter measured by the benchmark calibration. Performing the benchmark calibration at the beginning and the examined calibration at the end of the experiment, the system drift can be quantitatively defined. In the ideal case, both calibrations benchmark and examined, are equal and the error bounds $|S_{ij}-S_{ij}'|$ are zero.

To characterize calibration lines, the procedure proposed in [6] was used: the resistance R of the load standard can be measured using the 4-terminal method. Then, the first-tier multiline thru-reflect-line (TRL) [7] can be performed, setting the calibration reference impedance to the characteristic impedance Z_0 of the alumina lines used. The frequency range where the tested lines are no longer dispersive and, on the other hand, the load reactance is negligible can be used to extract the value of the line capacitance C. Once the line capacitance C is found, the characteristic impedance, the attenuation and relative phase constants can be extracted with the help of the MultiCal® software package.

Knowing the electrical parameters of the calibration thru and line standards, it is possible to set the position of the measurement reference plane and the measured reference impedance accurately with the help of the multiline TRL. Therefore, the benchmark calibration can be defined and verification of accuracy of the tested lumped calibration can be performed at different temperatures [2].

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III. Experimental Results

The experimental setup included a thermal probe system, an Agilent 8510C 50 GHz vector network analyzer (VNA), 50GHz GSG |**Z**| Probes with 150 µm pitch from SUSS MicroTec and 50 GHz GSG 100 µm pitch probe from another vendor (probe 'P'), and SussCal® and MultiCal® software packages. Commercially available alumina calibration substrates CSR-8 from SUSS MicroTec and substrate 'I' from another vendor were examined.

TABLE I
Measured Load Resistance

Temperature, °C	R, Ω (CSR-8)	R, Ω (Sub. 'I')
RT	49.99	49.96
50	49.99	50.02
100	50.05	50.29
150	50.09	50.54

To avoid additional uncertainty due to contact repeatability, all data were acquired in one measurement series in raw format with the help of the calibration software SussCal® and saved externally for the further analysis.

The experimental data included measurement results of all calibration standards that are required for the lumped (i.e. SOLT[1] or LRM+[2]) as well as for the multiline TRL calibrations. The measurement experiments were repeated at four different temperatures: at room temperature (RT), 50°C, 100°C, and 150°C for both calibration substrates and with the use of two different wafer probes (|**Z**| Probe and probe 'P'). The experiment took approximately four hours for the entire measurement cycle.

First, the drift of the experimental setup was determined using the procedure [10].

Next, the temperature stability of the load standard resistance was measured. As it was discussed in [2], the precise value of the load resistance is required for the accurate characterization of the line standard as well as for the lumped calibration at different temperatures. It was found that the temperature stability of the CSR-8 load resistance is better than 0.18%. The load of the substrate 'I' is less stable and showed a variation in its resistance within 1.08% (see Table I, Fig. 1).

The temperature dependence of the attenuation and relative phase constants of the line standards were extracted for each calibration substrate using the method [6]. Fig. 2 shows the loss and the relative phase constant of the CSR-8 line standard extracted at room temperature and 150°C. As it was expected, these parameters did not depend on the type of the wafer probe used. Fig. 3 and Fig. 4 demonstrate results for the whole temperature range for CSR-8 and substrate 'I' respectively.

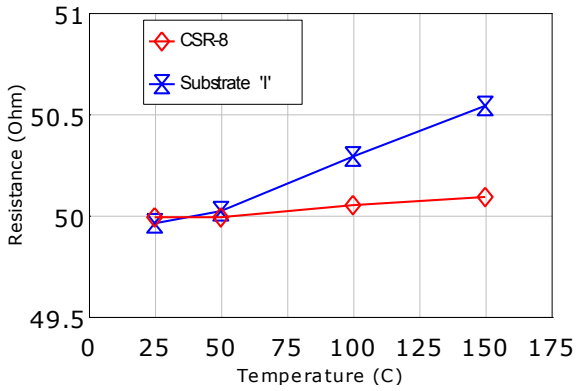

Fig. 1. Temperature stability of the load resistance of the CSR-8 and substrate 'I'. The load of the CSR-8 demonstrated stability better than 0.18% compared to 1.08% for the load of substrate 'I'.

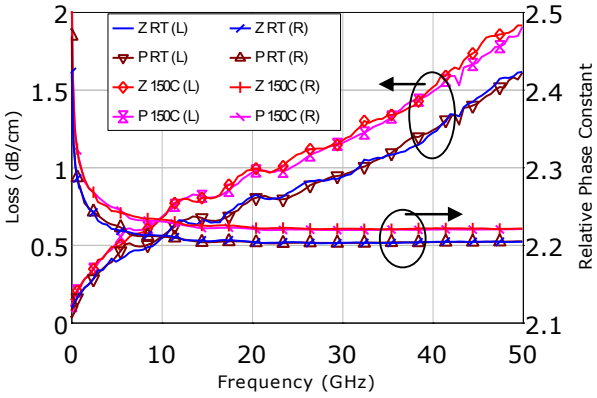

Fig. 2. Temperature stability of the line loss and relative phase constant of the CSR-8 calibration substrate measured with |**Z**| Probes and alternative probes 'P'. Comparison results are presented at room temperate (RT) and 150°C.

Observed changes in the line's loss and phase constant can lead to significant calibration and finally measurement errors of the lumped calibration if no additional correction procedure is applied.

To evaluate the worst-case influence of the line thermal instability on the lumped calibration, the following procedure was used. The equivalent model of the load on substrate "I" was extracted with respect to the multiline TRL calibration. The load series inductance was L=7.8 pH.

[1] Short-Open-Load-Thru
[2] Line-Reflect-Match, advanced

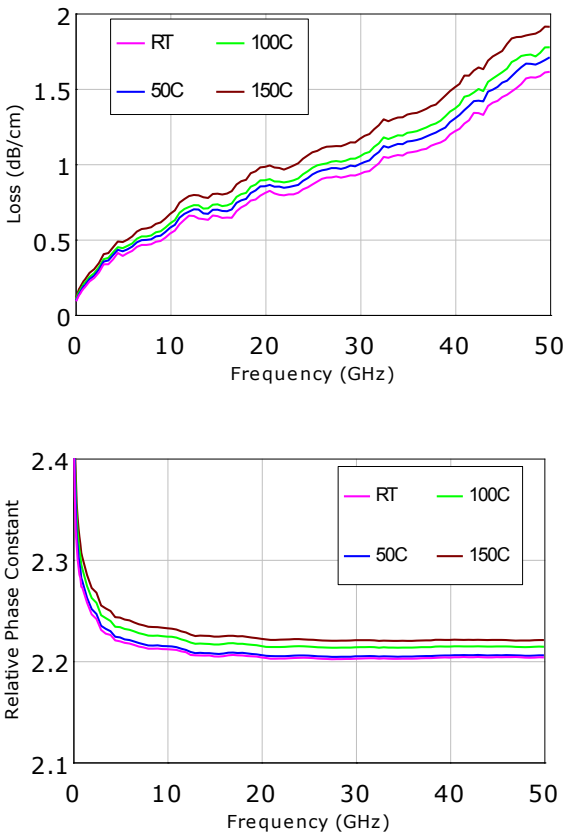

Fig. 3. Temperature stability of the line loss and relative phase constant of the CSR-8 calibration substrate as measured with |**Z**| Probes.

Next, the examined ("working") lumped LRM+ calibration was performed for the data series measured at room temperature and 150°C for both calibration substrates. For this calculation run, the thru standard was assumed to be lossless and perfectly matched. This is a conventional assumption used very often in practice. The lumped calibration accuracy was compared to the benchmark multiline TRL [2, 10]. The measurement reference plane was defined at the middle of the thru standard.

Finally, the temperature variation of the attenuation and the relative phase constants was included in the line model and the same calculations were repeated. Fig. 5 shows selected results from the experiment.

The worst-case 150°C experiment proved that the error of the high-temperature lumped calibration can be significantly decreased by improving the model of the used line standard and by taking its temperature instability into account. Therefore, the error in the calibration at 150°C was able to be corrected to that of the calibration at room temperature. In addition, it was observed that the results obtained from the CSR substrate were almost matched to the system drift. This was, however, not the case for the alternative substrate. Other factors must be taken into account in order to correct for this difference. One of these factors could be the difference in the line's characteristic impedance, which was not considered in this experiment.

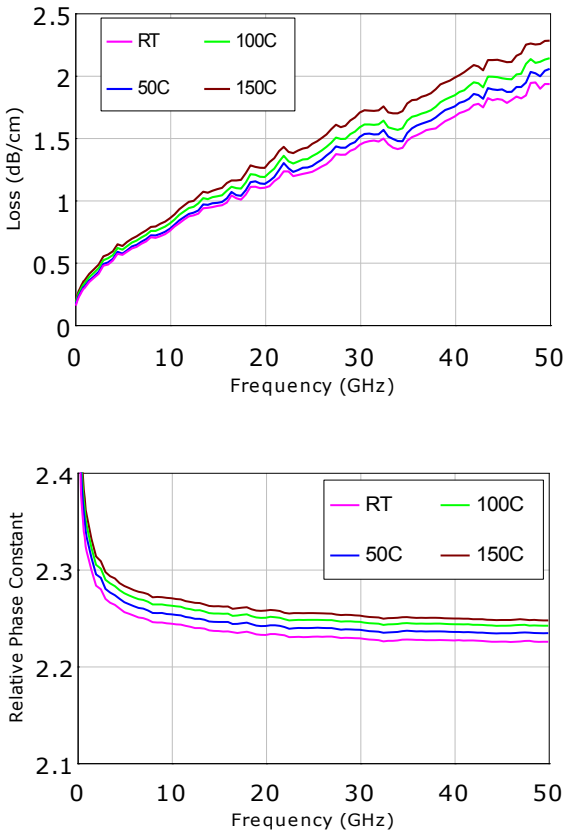

Fig. 4. Temperature stability of the line loss and relative phase constant of the alternative calibration substrate 'I' measured with |**Z**| Probes.

IV. Conclusion

Summarizing, for the first time a quantitative verification of the calibration and measurement accuracy at high temperatures was done. It was demonstrated that the temperature changes in the measurement setup leads to an increased measurement error. Obviously, the system should be re-calibrated at each temperature in order to achieve high measurement accuracy.

A practical method for characterizing the coplanar calibration thru and line standards at high temperatures was presented and verified for different commercially available alumina substrates up to 150ºC. Temperature dependent line, attenuation and relative phase constants were extracted for

each substrate. Comparison of the lumped and distributed calibration was done with and without compensation for the temperature variation of calibration standards.

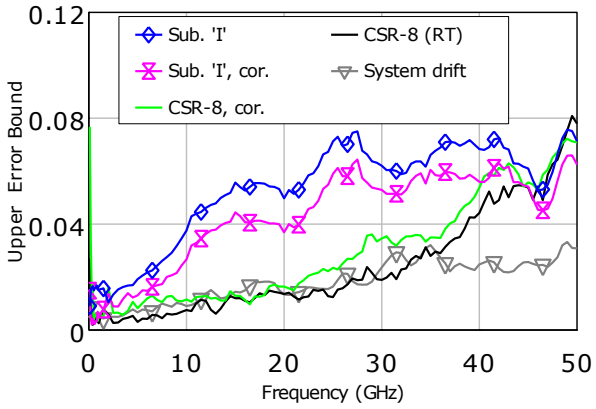

Fig. 5. Accuracy verification of the 150°C lumped calibration for both substrates "I" and CSR-8 with (red and green) and without (blue) correction for line temperature instability. The accuracy of room temperature calibration (black) on the CSR-8 is also shown.

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17.3 Paper [90]: “Sensitivity analysis of wafer-level over-temperature RF calibration”

A. Rumiantsev, G. Fisher, and R. Doerner, "Sensitivity analysis of wafer-level over-temperature RF calibration," in *Microwave Measurement Symposium (ARFTG), 80th*, San Diego, CA, USA, 2012, pp. 1-3.

This paper analyzed the commonly used wafer-level S-parameter calibration methods LRRM, multiline TRL and LRM+ for the sensitivity to the thermal variation of electrical characteristics of planar calibration standards. It was demonstrated that the calibration error of lumped-standard based methods could be significantly reduced by taking into account the variation of load standard resistance over the temperature. The obtained results proved that for the evaluated commercially available calibration standards and for a given frequency range, the overall calibration error due to the temperature variation was in order of magnitude of repeatability of the manual system calibration. The proposed method can be successfully applied for different calibration substrates, temperature and frequency ranges, as well as to the *in-situ* calibration element.

For this paper, I defined the scope of the work, develop the concept of the investigation, did several calculations, performed the data analysis, and wrote the major part of the paper. Ralf Doerner from Ferdinand-Braun-Institut (FBH), Leibniz-Institut fuer Hoechstfrequenztechnik (Berlin, Germany FBH, Berlin) acquired all measurement results at the FBH facility, did the major part of calculation as well as data analysis. Gavin Fisher from Cascade Microtech (Beaverton, OR, USA) contributed to some calculation tasks as well as to the preparing the final manuscript.

Sensitivity Analysis of Wafer-Level Over-Temperature RF Calibration

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***Abstract* — This paper analyzes the commonly used wafer-level S-parameter calibration methods LRRM, multiline TRL and LRM+ for the sensitivity to the thermal variation of electrical characteristics of planar calibration standards. We demonstrate that the calibration error of lumped-standard based methods can be significantly reduced by taking into account the variation of Load standard resistance over the temperature. The obtained results proved that for the evaluated commercially available calibration standards and for a given frequency range, the overall calibration error due to the temperature variation is in order of magnitude of repeatability of the manual system calibration. The proposed method can be successfully applied for different calibration substrates, temperature and frequency ranges, as well as to the *in-situ* calibration element.**

***Index Terms* — S-parameter calibration, device characterization, mm-wave measurements, on-wafer calibration.**

I. Introduction

Continually increasing demand for more data, more content and high speed pushes operation frequencies of modern RF circuits towards mm-wave and sub-THz ranges. Circuit designers challenge modeling engineers for more accurate device models, optimized and verified at extremely wide frequency range, across multiple temperatures and with the highest level of accuracy. Development of accurate and consistent wafer-level S-parameter calibration methods covering wide frequency and temperature ranges becomes the critical success factor.

While some work has been already done in this area (e.g. [1]), to the best of author's knowledge, the quantitative analysis of contribution of a selected calibration standard to the overall accuracy of over-temperature S-parameter calibration methods is not yet available. Practical recommendations on how to address the variation of electrical properties of standards across wide temperature range are still missing.

In this work, we evaluated the sensitivity of the most popular wafer-level self-calibration procedures, such as multiline TRL[1] [2], enhanced LRRM[2] [3] and LRM+[3] [4] to the variation of electrical characteristics of coplanar calibration standards due to the temperature change. The objective of this work was to identify the method that provides the smallest calibration residual errors for a given set of conditions.

II. Analysis Method

Multiline TRL, eLRRM and LRM+ calibration methods differently define calibration reference impedance Z_{REF}. For the multiline TRL, the reference impedance is set to the characteristic impedance Z_0 of the Line standard. Assuming that the dielectric loss of the evaluated alumina calibration substrate is negligible in the frequency range of interest, we calculated Z_0 from the measured capacitance per unit length C' and propagation constant γ, as proposed in [5, 6]. Once Z_0 is known, the calibration reference impedance can be transformed to the desired value of $Z_{REF} = 50\ \Omega$.

The Z_{REF} for eLRRM and LRM+ depends on the impedance of the Load Z_{LOAD} as well as Z_0 and γ of the Thru. Therefore, multiline TRL, eLRRM and LRM+ may show different calibration residual error across the temperature range.

We chose the maximum error bounds for measured S-parameters of a passive device as the figure of merit (FoM) of the calibration accuracy, calculated by the comparison technique [7]. As demonstrated in several previous works (e.g. [8, 9]), the resistance of a coplanar Load standard R_{LOAD} as well as the propagation constant γ are affected by the variation of the Impedance Standard Substrate (ISS) temperature. As a result, the accuracy of the probe tip calibration varies across the temperature range.

To quantify this variation, we measured the resistance of the Load standard R_{LOAD} and extracted the propagation constant γ as well as the capacitance per unit length C' of the Line at each temperature point, including room temperature.

The attenuation coefficient α_{REF} used for the Thru model in lumped-standard based calibration methods, such as eLRRM and LRM+ was extracted from propagation constant:

$$\alpha(f) = \alpha_{REF} \frac{\tau}{\tau_{REF}} \sqrt{\frac{f}{f_{REF}}} \qquad (1)$$

where: α_{REF} is the attenuation of the reference element, dB extracted at the reference frequency f_{REF}, Hz; τ is the electrical delay of the Thru standard, sec; τ_{REF} is the delay of the reference element, sec; f is the measured frequency, Hz.

[1] Thru-Reflect-Line

[2] Line-Reflect-Reflect-Match

[3] Line-Reflect-Match, advanced

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For instance, the reference element for the evaluated ISS model 104-783A is the 27 pico-second long Line.

To avoid additional uncertainty due to contact repeatability, all data were acquired in one measurement series and saved for the further analysis.

Next, different sets of error terms were calculated for $R_{LOAD}(T)$, $\alpha_{REF}(T)$, $Z_0(T)$ (for eLRRM and LRM+) and $C'(T)$ (for multiline TRL) for measurement data taken at a certain temperature as:

1) *Benchmark*. T is the measurement temperature;
2) *Worst case*. $T = 25°C$ (room temperature).

Further, we calculated error sets for configurations where only a single standard parameter was corrected for the temperature impact. This should show the proportional impact of the selected parameter on the overall calibration accuracy.

III. Experimental Results

The experimental setup included a manual thermal probe system from Cascade Microtech, and Agilent 8510C 50 GHz vector network analyzer (VNA). WinCal XE calibration software from Cascade Microtech was used for measuring S-parameters of standards, calibration and analysis.

Extracted parameters of calibration standards are summarized in Table 1. Fig 1 shows the attenuation constant α extracted from the multiline TRL as well as its model approximated by (1). α_{REF} increases with the temperature by 0.1 dB (or 18%) at $T = 150°C$ compared to nominal (room temperature) value.

C' also increases by 0.025 pF/cm resulting in a decrease of Z_0 by 0.38 Ω (or 0.8%) and 0.07 Ω (or 15%) for its real and imaginary parts respectively. Fig. 2 shows Z_0 calculated from a known C' and γ.

TABLE I
Standard Parameters Variation over Temperature

Parameter	Temperature, C			
	+25	+50	+100	+150
α_{REF} @ 40 GHz, dB	0.56	0.59	0.62	0.66
C', pF/cm	1.560	1.565	1.575	1.585
$\Re(Z_0)$ @ 40 GHz, Ω	47.71	47.66	47.47	47.33
$\Im(Z_0)$ @ 40 GHz, Ω	-0.46	-0.47	-0.50	-0.53
R_{LOAD}, Ω	49.94	50.07	50.32	50.55

Once $Z_0(T)$, $\alpha_{REF}(T)$, and $R_{LOAD}(T)$ are defined, the impact of each of them on the calibration accuracy can be calculated.

The maximum error bounds for the multiline TRL, eLRRM and LRM+ were calculated at three temperature points: $T = 50°C$, $T = 100°C$, and $T = 150°C$ (Fig. 3). The maximum error of 2.4% at 50 GHz corresponds to the worst-case multiline TRL for $C'(25°C)$ and $T = 150°C$. Both eLRRM and LRM+ have comparable errors of about 2.2% for the worst-case scenario of $T = 150°C$, $R_{LOAD}(25°C)$, $Z_0(25°C)$, $\alpha_{REF}(25°C)$.

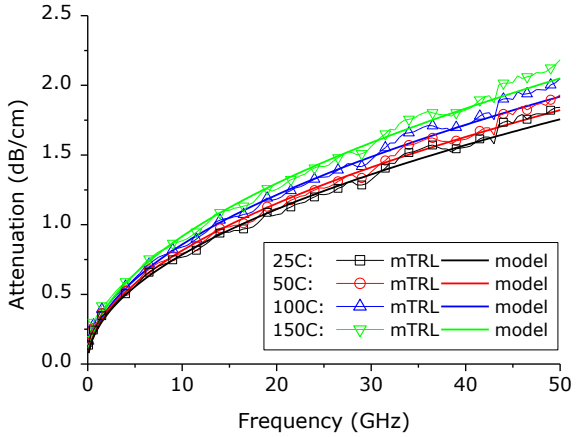

Fig. 1. Attenuation constant of the CPW Line standard measured across the temperature and approximated by (1).

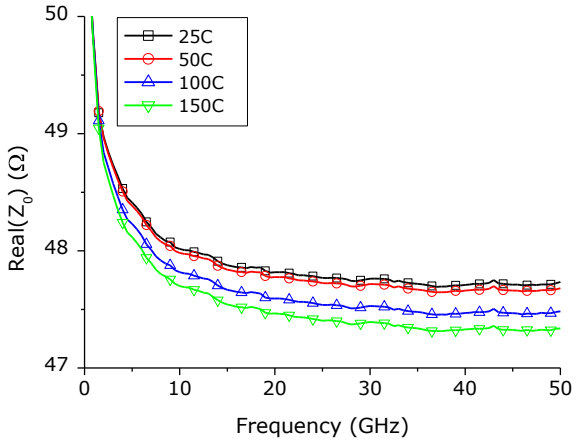

Fig. 2. Real part of the characteristic impedance Z_0 of the CPW Line standard measured across the temperature.

Last, we calculated the impact of each standard parameter on the accuracy of eLRRM (Fig. 4). Results showed that the resistance of the Load R_{LOAD} is the most influencing factor for the evaluated ISS. Thus, addressing its temperature variation reduced overall calibration error from 2.2% down to negligible value of 0.6%. Correction for α_{REF} and Z_0 had marginal effect.

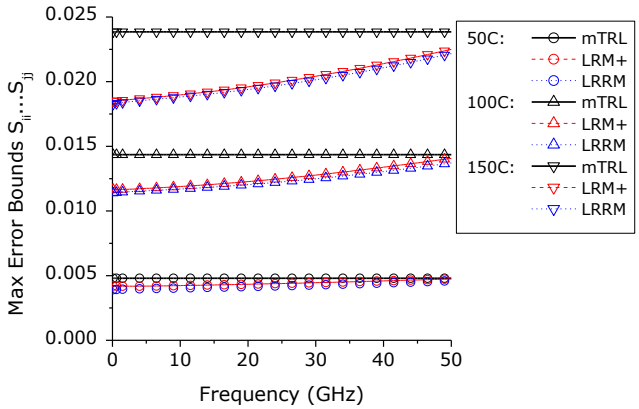

Fig. 3. Maximum error bounds calculated for multiline TRL, eLRRM+ and LRM+ for $T_1 = 50°C$, $T_2 = 100°C$, and $T_3 = 150°C$ with benchmark and worst case definition of standard properties.

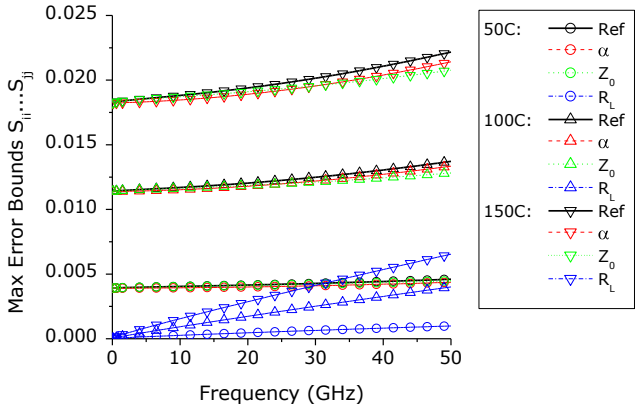

Fig. 4. Maximum error bounds for eLRRM calibration procedure for $T_1 = 50°C$, $T_2 = 100°C$, and $T_3 = 150°C$ calculated individually for the benchmark definitions of the Load resistance R_{LOAD}, the loss α_{REF} or the characteristic impedance Z_0.

IV. Conclusion

Sensitivity analysis of the wafer-level over-temperature calibration was performed for commonly-used methods: multiline TRL, eLRRM, and LRM+. This investigation was focused on a commercially available alumina Impedance Standard Substrate.

The obtained results demonstrated that temperature variation of the electrical characteristics of Load and Thru standards leads to different calibration residual errors depending on the calibration method used.

For the considered experimental setup, we found that the lumped-standard based calibration methods were less sensitive to temperature. In addition, the Load resistance R_{LOAD} is the main influencing factor for both eLRRM and LRM+ methods. Therefore, a simple correction for $R_{LOAD}(T)$ can significantly improve calibration accuracy.

The proposed method can be successfully applied for other types of calibration substrates, temperature and frequency ranges, as well as to the *in-situ* (on-wafer) calibration elements.

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17.4 Paper [93]: “Impact of in-situ TRL reference impedance determination on parameter extraction”

A. Rumiantsev, R. Doerner, and F. Lenk, "Impact of in-situ TRL reference impedance determination on parameter extraction," in *European Microwave Conference, 42nd,* Amsterdam, NL, 2012, pp. 593-596.

This paper investigated the impact of possible parameter extraction errors caused by inaccurate definition of the calibration reference impedance of *in-situ* multiline TRL. Two calibration sets implemented on GaAs and Si/SiGe:C wafer processes were quantitatively analyzed. Obtained results demonstrated that for most practical cases, the desired 5%-level of confidence of extracted parameters of high-reflective devices can easily be achieved without additional efforts. Thus, implementation of the *in-situ* TRL into a characterization workflow of high-performance microwave devices can be significantly simplified.

For this paper, I developed the analysis methodology, planned the work, acquired data for the BiCMOS process, did a part of calculations and parameter extraction, and wrote the major part of the paper. I performed the data analysis together with Ralf Doerner from Ferdinand-Braun-Institut (FBH), Leibniz-Institut fuer Hoechstfrequenztechnik (Berlin, Germany). Ralf Doerner acquired data for GaAs process and did the major part of calculations. The access to the GaAs test structures was provided by Friedrich Lenk from Hochschule Lausitz (FH) (Senftenberg, Germany).

Impact of *in-situ* TRL Reference Impedance Determination on Parameter Extraction

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***Abstract*—This paper investigates the impact of possible parameter extraction errors caused by inaccurate definition of the calibration reference impedance of *in-situ* multiline TRL. Two calibration sets implemented on GaAs and Si/SiGe:C wafer processes were quantitatively analyzed. Obtained results demonstrated that for most practical cases, the desired 5%-level of confidence of extracted parameters of high-reflective devices can easily be achieved without additional efforts. Thus, implementation of the *in-situ* TRL into a characterization workflow of high-performance microwave devices can be significantly simplified.**

Keywords—component; S-parameter; calibration; on-wafer measurements; HBT

I. INTRODUCTION

The continuous increase of operation frequencies of advanced microwave devices (e.g. [1, 2]) causes serious device characterization challenges. Wafer-level measurement systems must provide more accurate, reliable and repeatable calibration and measurement results at mm and sub-mm frequencies.

Wafer-embedded (*in-situ*) calibration techniques have already demonstrated substantial advantages over conventional probe pad de-embedding at mm-wave frequencies [3-6]. Implementing customized standards on-wafer allows for capturing the major part of device backend parasitics and for moving the measurement reference plane close to the DUT terminals in one step [7]. Therefore, with increasing of measurement frequency, *in-situ* calibration becomes an effective tool.

However, its practical realization suffers from some difficulties:

- A certain number of electrical parameters of calibration standards must be known, such as characteristic impedance Z_{LINE} of the Line or the impedance Z_{LOAD} of the Load [3].
- Process instability and fabrication tolerances affect the accuracy of standards. Therefore, each calibration chip should be characterized before use.
- Conventional S -parameter measurement systems are not necessarily equipped with instruments that may be required for accurate characterization of customized standards (e.g. precision impedance analyzers).

That is why *in-situ* calibration is still not widely implemented into a device characterization workflow.

This work investigates the impact of characteristic impedance Z_{LINE} of *in-situ* multiline TRL[1] [8] on parameter extraction accuracy of passive and active devices. The test chips were implemented in a passive GaAs process from FBH and in advanced Si/SiGe:C ST Microelectronics' BiCMOS9MW process technologies [1]. Z_{LINE} was characterized over measured capacitance per unit length C' and propagation constant γ of the Line. Obtained results demonstrate that, in most cases, the desired 5%-level of confidence in parameter extraction of passive and active devices can be easily achieved on conventional S -parameter characterization setup without additional efforts.

II. DESIGN AND IMPLEMENTATION

A. GaAs Calibration Standards

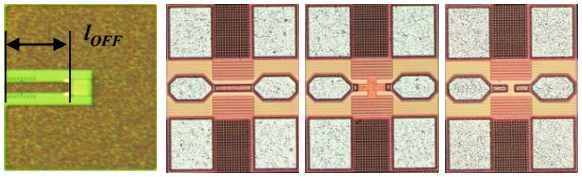
The achievements made over the past years in fabricating and characterizing custom calibration standards on semi-insulating and conductive wafer processes established a solid background for accurate *in-situ* calibration [7, 9].

All GaAs calibration standards and DUTs utilize the same ground-signal-ground (GSG) RF contact pad design. They are realized on semi-isolated 625 µm GaAs substrate with 3 µm electroplated Au metallization as top metal layer in coplanar

[1] Thru-Reflect-Line

configuration. The process also includes NiCr thin-film resistors and air-bridges.

The contact pad is realized by a 50 Ω coplanar line with a center and slot width of 20 µm and 15 µm, respectively. The half-length of the Thru offset l_{OFF} of 100 µm (Fig. 1, a) is used for Short, Open, and Load. The offset ensures a sufficient separation of the probes and a well-guided coplanar mode. A nonius is added to every contact pad for precise definition of the probe overlap of 25 µm and for repeatable probe placement. The Line length varies from 480 µm to 9400 µm to cover the frequency range from 500 MHz to 110 GHz.



a) b) c) d)

Figure 1. The offset Load implemented on GaAs test chip (a). Thru, Short and Open implemented on the SiGe test chip (b)-(d).

B. SiGe Calibration Standards

SiGe standards and DUT utilize the same GSG RF contact pad configuration as the GaAs test chip. Metal 1 (M1) ground shield eliminates the losses in a resistive substrate and makes the parasitics of the pads purely capacitive. The signal pads consist only of the upper Metal 6 (M6) minimizing the parasitic pad capacitances to the ground. The pad size is reduced to the smallest possible dimension.

The calibration standards are designed as a M1-shielded 50 Ω top metal grounded coplanar waveguide. The effective length was optimized to cover the frequency range from 1 GHz to 110 GHz and yielded 51, 549, 1545 and 3039 µm for the Thru and Lines, respectively. The symmetrical Short element is located at M6. The Open and the Thru have the same offset (Fig. 1).

C. Calibration Reference Impedance

As shown in [10], multiline TRL sets the calibration reference impedance Z_{REF} to the characteristic impedance of the Line Z_{LINE}. Because planar waveguides are dispersive and affected by fabrication inaccuracies, it is required to measure Z_{LINE} accurately and to transfer the TRL calibration reference impedance to the desired value of $Z_{REF} = 50\,\Omega$. The simple "lumped load" method of Z_{LINE} measurement over the line capacitance per unit length C' for semi-insulating wafers was introduced in [11]. For proper designed standards, it can also be applied for conductive wafers, as shown in [12]. Thus, C' can be extracted from:

$$C' \approx \Re\left(\frac{\gamma}{j\omega R_{LOAD}}\frac{1+\Gamma_{LOAD,Z_{LINE}}}{1-\Gamma_{LOAD,Z_{LINE}}}\right) \qquad (1)$$

where γ is the propagation constant of the Line. It can be directly extracted from the TRL algorithm. $\Gamma_{LOAD,Z_{LINE}}$ is the reflection coefficient of the Load, measured with respect to the calibration reference impedance Z_{LINE}. R_{LOAD} is Load resistance.

From:

$$\frac{\gamma}{Z_{LINE}} = j\omega C' + G' \qquad (2)$$

and, assuming that $G/\omega C$ is negligible:

$$Z_{LINE} \approx \frac{\gamma}{j\omega C'} \qquad (3)$$

Once Z_{LINE} is defined, the measurement results can be transformed to any desired reference impedance Z^n_{ref} (which is, in general, complex) over T -parameters [10] by:

$$T^{nn} = Q^{nm}T^{mm}Q^{mn} = \frac{1}{1-\Gamma^2_{nm}}\times$$
$$\times\begin{pmatrix}1 & \Gamma_{nm}\\ \Gamma_{nm} & 1\end{pmatrix}T^{mm}\begin{pmatrix}1 & -\Gamma_{nm}\\ -\Gamma_{nm} & 1\end{pmatrix}, \qquad (4)$$

where T^{mm} and T^{nn} are T -parameter matrices of the DUT for reference impedances Z^m_{ref} (source) and Z^n_{ref} (target), respectively. Γ_{nm} is defined as:

$$\Gamma_{nm} \equiv \frac{Z^m_{ref} - Z^n_{ref}}{Z^m_{ref} + Z^n_{ref}}. \qquad (5)$$

III. Experimental Results

A. Measurement Setup

The experimental measurements were carried out on a broadband S -parameter measurement system from Cascade Microtech, consisting of a manual PM8 probe station, 100 µm pitch Infinity probes model SP-i110-A-GSG-03, and equipped with the 110 GHz PNA network analyzer from Agilent Technologies and the source monitor unit (SMU). The measured data are acquired in raw format (with the S -parameter calibration turned off). Calibration and error correction were performed for the same data set outside of the VNA on a computer. We used WinCal XE®[2], MultiCal®[3], and proprietary MATLAB®[4] script for this purpose, while device parameters were extracted using MATLAB.

B. Measurement of Line Characteristic Impedance

The multiline TRL was performed on both SiGe and GaAs test chips for $Z_{REF} = Z_{LINE}$ and the reflection coefficient $\Gamma_{LOAD,Z_{LINE}}$ was calculated. The SMU (connected to the mm-wave test heads bias-Ts) was used to measure R_{LOAD} through RF probes. The test port resistance was defined using the Short standard and subtracted from the measured R_{LOAD}.

[2] Commercially available from Cascade Microtech, Inc.
[3] Available from NIST
[4] Commercially available from MathWorks, Inc.

While the Load was designed for $R_{LOAD} = 50\,\Omega$, process fabrication inaccuracies caused a deviation of 2.4 Ω for SiGe and 11.1 Ω for GaAs Load (Table 1).

(1)-(3) show that ill-defined R_{LOAD} leads to inaccurate C' and Z_{LINE}. With the help of a mathematical model, error bounds for C', Z_{LINE} as well as for the extracted parameters of DUT were calculated for a given worst-case error in R_{LOAD} of 10%. (Fig. 2, Table 1). Table 1 gives the real and imaginary parts of the Z_{LINE} extracted at 10 GHz.

TABLE I. EXTRACTED PARAMETERS OF LINES

	Measured/ Extracted Parameter		
	Nominal value	***Lower bound***	***Upper bound***
Si/SiGe: C Process			
R_{LOAD}, Ω	47.6	42.84	52.36
C_{LINE}, pF/cm	1.259	1.399	1.144
Re(Z_{LINE}), Ω @10 GHz	51.12	46.00	56.23
Im(Z_{LINE}), Ω @10 GHz	-3.07	-2.86	-3.39
GaAs Process			
R_{LOAD}, Ω	61.1	55.0	67.2
C_{LINE}, pF/cm	1.725	1.917	1.568
Re(Z_{LINE}), Ω @10 GHz	47.69	42.92	52.46
Im(Z_{LINE}), Ω @10 GHz	-1.34	-1.20	-1.47

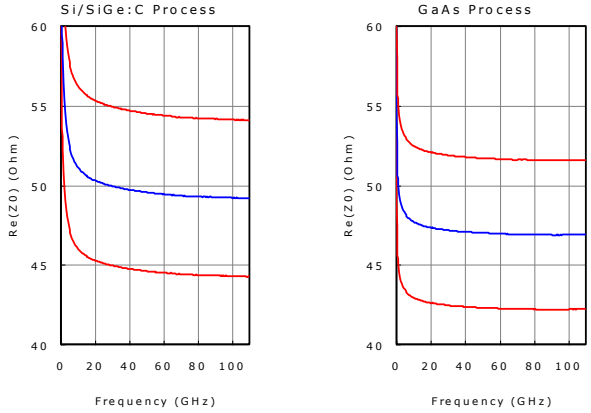


Figure 2. Real part of the extracted characteristic impedance Z_{LINE} (blue) and measurement error bounds (red) from Si/SiGe:C (left) and GaAs (right) processes.

C. Results for Passives

The passive GaAs test chip included the offset Short with a serial inductance $L_{SHORT,GaAs}$ of about 31.5 pH and the Open exhibiting a parallel capacitance $C_{OPEN,GaAs}$ of about 14 fF. The measured S-parameters of these elements were corrected with respect to multiline TRL for $Z_{REF} = Z_{LINE}$. Next, the results were transformed to $Z_{REF} = 50\,\Omega$ using (4) for nominal, upper and lower bounds of Z_{LINE} (±10% error for R_{LOAD}). Equivalent capacitances of the Open and inductances of the Short where extracted from the Π - and the T-equivalent circuits, respectively. Figure 3 shows the port 1 capacitance $C1$ of the Open and Port 1 inductance $L1$ of the Short, normalized to nominal values. Even for worst-case bounds for R_{LOAD} of 10% from the nominal value of 61.1 Ω, the calculated extraction errors are within -9%...+11% for capacitance $C1$ and +/-10% for inductance $L1$ (Fig. 3, red lines). Parameters that were extracted without re-normalization of the reference impedance from Z_{LINE} to $Z_{REF} = 50\,\Omega$ are also within this region: -4.5% @ 10 GHz for $C1$ and +4.9% @ 10 GHz for $L1$ (Fig. 3, green diamonds). Results for other elements are comparable.

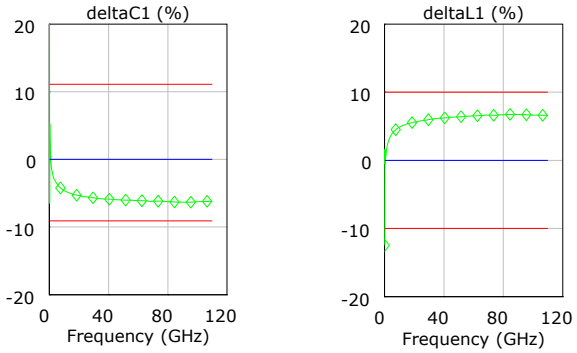


Figure 3. Error bounds for Port 1 capacitance $C1$ of the Open (left) and Port 1 inductance $L1$ of the Short (right) of GaAs test chip, normalized to nominal values. Nominal values are extracted from $Z_{REF} = 50\,\Omega$ (blue). Green diamond curve corresponds to $Z_{REF} = Z_{LINE}$.

D. Active DUT Results

An HBT with 14.86 µm length and 0.12 µm emitter stack available from BiCMOS9MW process was measured in a cold-S mode with $V_B = 0$ V…+1 V and $V_C = 0$ V and in hot-S (active) mode with $V_B = 0.7$ V…+1 V and $V_{CB} = 0$ V (emitter grounded in both cases). Important figures of merits (FoM), such as C_{BC}, C_{BE}, f_T and f_{MAX} were extracted. For this experiment, the calibration reference plane was kept at the M6 (top metal) level.

The extracted nominal value of C_{BE} is 26.5 fF[5]. For the worst-case error bounds of 10% for measured R_{LOAD} of 47.6 Ω, the errors for C_{BE} are within -9%...+11% (Fig. 4, red lines). It is only 2% @10 GHz without re-normalization of the reference impedance, e.g. for $Z_{REF} = Z_{LINE}$ (Fig. 4, green diamonds).

[5] Because the calibration reference plane is set to M6, C_{BE} also includes via parasitic inductance and M6-M1 parasitic capacitance.

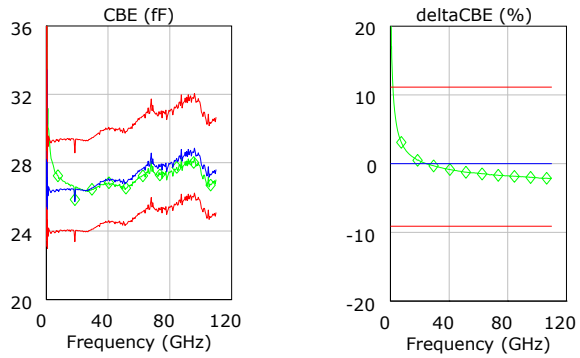


Figure 4. The absolute(left) and normalized (right) results for base-emitter capacitance of a test Si/SiGe:C HBT at V_{BE} = 0V for Z_{REF} = 50 Ω (blue), $Z_{REF} = Z_{LINE}$ (green diamonds) and estimated error bounds (red). The measurement reference plane is set to the M6 (top metal).

IV. Conclusion

A quantitative accuracy analysis of *in-situ* multiline TRL calibration implemented in both semi-insulating and conductive wafers was performed. The impact of possible measurement errors of R_{LOAD} on extraction of C' and Z_{LINE} was estimated. The measurement error bounds for extracted parameters of passive and active DUTs were calculated for a worst-case error in R_{LOAD}. Obtained results showed that the I-V measurement capability (provided by SMU) of a conventional S -parameter characterization setup is sufficient for accurate extraction of C' and Z_{LINE} of customized Line standards.

It was also shown, that Z_{LINE} stays within the desired level of confidence even at low frequencies for proper layout of the Line. For such cases and when characterizing high-reflective DUTs, the extraction of Z_{LINE} and the re-normalization of the TRL reference impedance to 50 Ω may not be required. Thus, implementation of the *in-situ* TRL into a characterization workflow of high-performance microwave devices can be significantly simplified.

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18 ATTACHMENT TO CHAPTER 9

18.1 Paper [109]: “The modified ripple test for on-wafer S-parameter measurements"

H. Heuermann and A. Rumiantsev, "The modified ripple test for on-wafer S-parameter measurements," in *ARFTG Microwave Measurements Conference-Spring, 69th,* 2007, pp. 1-5.

This paper addressed the background, implementation, and the on-wafer measurement results of and automatic analysis of the accuracy of S -parameters. The classic ripple-test was automated and expanded to the use of a dispersive transmission line as a reference. For the first time a dispersive coplanar line standard was used for the ripple-test. The novel technique was demonstrated through a number of examples. Numerical and measurement results verified the proposed method.

In this work, I provided a list of requirements, planned the work, and made all measurements. I also calculated electrical characteristics of the reference coplanar line required for the algorithm. Prof. Holger Heuermann from Fachhochschule Aachen (Aachen, Germany) implemented the impedance transformation step into the automated ripple test, did all calculations and wrote the major part of the paper. I presented this work at the ARFTG-69th conference.

The Modified Ripple Test for On-Wafer S-Parameter Measurements

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***Abstract*— This paper addresses the background, implementation, and the on-wafer measurement results of an automatic analysis of the accuracy of S-parameters. The classic ripple-test is automated and expanded to the use of a dispersive transmission line as a reference. Consequently, it was the first time a dispersive coplanar line was used for the ripple-test. The novel technique is illustrated through a number of examples. Numerical and measurement results have verified the proposed method.** [1]

I. Introduction

Many users of vector network analysers (VNAs) do not question their S-parameter measurements. Easily identifiable stochastic error is intrinsic because of the good repeatability and reproducibility of the VNA measurements the user often believes the results. However, every VNA-measurement includes errors. The non-ideal calibration standards (especially matched loads and opens) and the corresponding calibration method have strong influence on the measurement accuracy.

Experienced users are aware of the classic ripple test and apply it for evaluating the measurement accuracy of coaxial systems using an air-line as a reference, as shown in [1], [2]. More complex ways to estimate measurement errors are given in [3].

The ripple test is a simple calculation of the worst case estimates of S-parameter measurement errors. However, for on-wafer measurements as well as for waveguide measurements, the classic ripple test is not practical: the reference transmission line is not ideal; it is lossy and typically dispersive.

This paper will demonstrate the modification of the classic ripple test for wafer-level applications and the measurement results obtained from a 110 GHz setup.

The new algorithm can handle dispersive and lossy lines. It also implements the source match estimation from [2] to automate the procedure and to calculate the error bars for reflection S-parameter measurements.

This paper is organized as follows: first, the classic ripple test is presented. Then, the automation of the ripple test is explained. Next, the implementation of the dispersive reference lines is presented. Then, experiments with synthetic measurements will demonstrate the precision of the algorithm. Finally, experimental measurement results verify the proposed method and is illustrated in a number of examples.

[1] ©ARFTG-spring-conference, Honolulu 2007

II. Sources of Measurement Errors

For every measurement, users would like to see the uncertainty in the measurement results approximated with the error bars, as shown in Fig. 1.

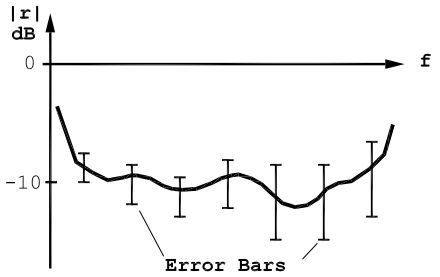

Fig. 1. Reflection measurement over frequency with error bars

The measurement errors of scattering parameter measurements with modern VNAs can be identified into two types: random errors and systematic errors.

Random errors over frequency can be identified very easily. The finite measurement dynamic of the VNA is an example. The repeatability of connections introduces errors in every measurement.

Often, the largest errors are systematic ones. In contrast to random errors, systematic errors can not be identified easily. Here the non-ideal calibration standards have the largest influence. Most problems come from matched loads and opens. Also the calibration method and/or its implementation can have an influence. An example is the old and new TRL-application. If the equations from [4] or [5] are used, error can be observed around the frequencies $n \cdot \lambda/2$ ($n = 0, 1, 2, ...$). By using [6], the error-areas are minimized. A comparison is illustrated in Fig. 2 with $n = 0, 1$.

Other sources of measurement errors are cable phase dispersion and temperature drift, [7].

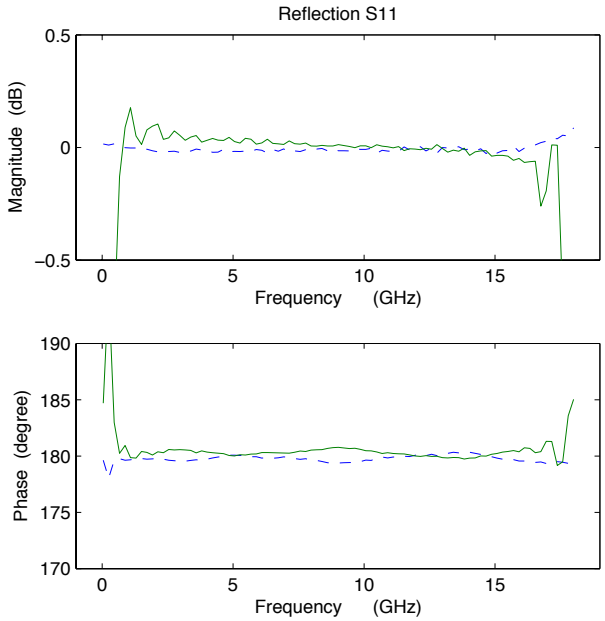

Fig. 2. Reflection coefficient of a short on a PTFE-substrate by using TRL from [5] (solid) and [6] (dashed)

III. The Classic Ripple Test

The classic ripple test can be used for small reflection measurement errors. It does not use the error coefficient of classic calibration procedures and is based on a simpler model.

The error of a VNA-measurement corresponds to the so-called source match with the error vector r_q, which is the vector between the real reflection vector r_w and the measured reflection vector r_m, as shown in Fig. 3.

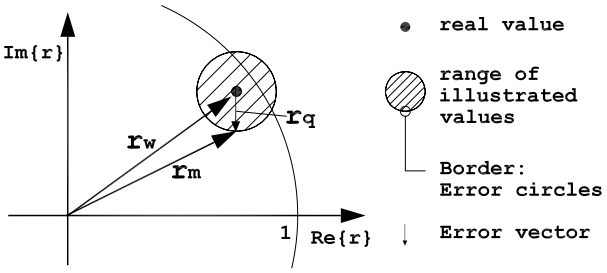

Fig. 3. Model: emergence of ripples in the r-plane

All errors are included in the final source match with the error vector r_q, the value to be identified. Fig. 4 shows the error model for the classic ripple test.

A measurement of a long, matched transmission line loaded with the short is needed to calculate the source match Z_q, which corresponds to the error vector r_q by:

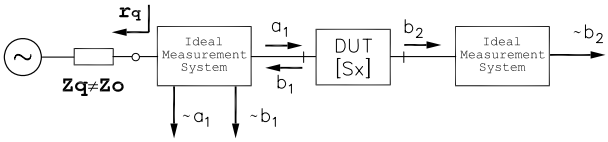

Fig. 4. VNA error model for the classic ripple test

$$r_q = \frac{Z_q + Z_0}{Z_q - Z_0} \quad . \tag{1}$$

Fig. 5 illustrates the measurement set-up for the classic ripple test to calculate the source match.

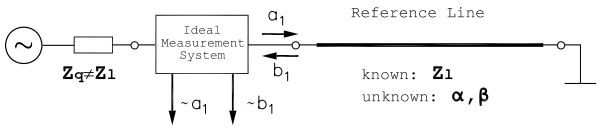

Fig. 5. Set-up to perform the r_q-calculation for the classic ripple test

In practice, the source impedance Z_q and the system impedance Z_0 are not the same for a real VNA measurement. The measurement of the reflection values of the long transmission line is shown in Fig. 6. Instead of

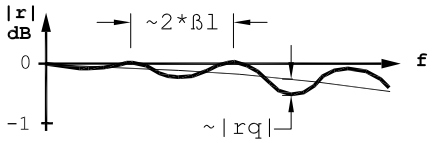

Fig. 6. Reflection results of a matched line loaded with the short for a real VNA measurement

showing an increase in the magnitude of reflection losses over the frequency sweep it shows a ripple response. The results should show only an increase of the losses over the frequency as an effect of the skin deep.

The mathematical approximation for the ripple test is based on Fig. 3. It can be approximated as:

$$r_m \simeq r_w + r_q \quad . \tag{2}$$

This approximation can be proved by the following equations:

$$r_w = \frac{Z_w + Z_0}{Z_w - Z_0} \quad , \tag{3}$$

$$r_m = \frac{Z_m + Z_0}{Z_m - Z_0} \quad , \tag{4}$$

with the approximation: $Z_q \simeq Z_0$.

The practical ripple test is performed in this way: first, measure the peak-to-peak ripple by using a long, matched line loaded with the short. Next, use a table (see [2]) to find the corresponding source match. Then, calculate the

so-called delta-match between the reflection value of the DUT and source match. Finally, use the delta-match from the table to find the corresponding magnitude and phase error.

In [2] a practical example is given along with the modified ripple test, which is necessary to automate the ripple test.

IV. Automation of the Ripple Test

The modified ripple test uses the model illustrated in Fig. 7 to measure the source match with the error vector r_q. Only the reflection value S_{11} is measured.

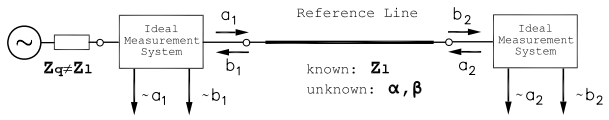

Fig. 7. Setup to measure the source match for the modified ripple test

Using the classic ripple test, it was only possible to estimate the source match for a few frequency points. The results are the average value for a frequency band of one ripple. So, it was necessary to use a very long line to have a lot of ripples.

The test of Fig. 7 works for every frequency point, except the areas around $n \cdot \lambda/2$ for $n = 0,1,2,....$ To overcome this problem, a multi-line solution can be chosen.

However, the line impedance Z_l of reference line must be similar to the system impedance Z_0, often $50\,\Omega$. Due to this fact, the classic or modified ripple tests can only be used in a line system with real TEM wave guides, e.g. coaxial lines.

V. Implementation of a Dispersive Reference Line

The dispersive characteristic of a coplanar line for on-wafer an calibration substrate[2] is shown in Fig. 8.

The line impedance was extracted using the procedure introduced in [8] and verified for commercial calibration substrates in [9].

In order to use a dispersive transmission line to estimate the source match, renormalization is necessary.

The Z-parameters were used for the renormalization. The so-called port impedance matrix

$$[\mathbf{Z_{La}}] = \begin{pmatrix} 50 & 0 \\ 0 & 50 \end{pmatrix} \tag{5}$$

is used for a reference to $50\,\Omega$. Port impedance matrices have the real or complex port impedance value in the trace. All other elements are zero.

[2]The CSR-8 calibration substrate from SUSS MicroTec was used.

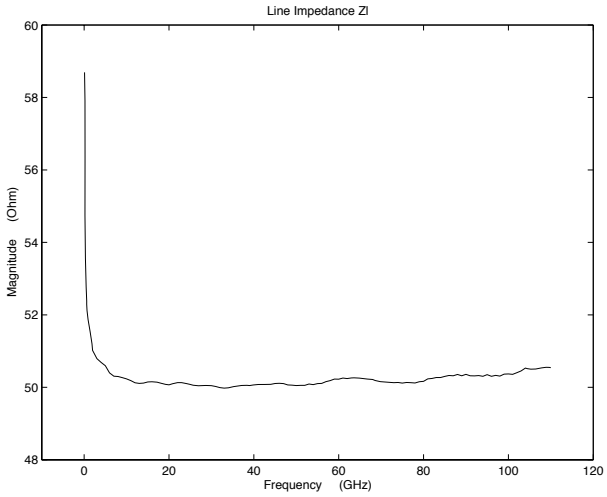

Fig. 8. Magnitude of impedance of the dispersive $50\,\Omega$ coplanar line on Al_2O_3-substrate

$[\mathbf{I}]$ is the unit matrix.

The first step is the calculation of the normalized matrix $[\mathbf{za}]$ from the measured S-parameter of the line:

$$nen = (1 - S_{11}) \cdot (1 - S_{22}) - S_{21}S_{12} \ , \tag{6}$$
$$za_{11} = ((1 + S_{11}) \cdot (1 - S_{22}) + S_{21}S_{12})/nen \ , \tag{7}$$
$$za_{12} = 2 \cdot S_{12}/nen \ , \tag{8}$$
$$za_{22} = ((1 - S_{11}) \cdot (1 + S_{22}) + S_{21}S_{12})/nen \ , \tag{9}$$
$$za_{21} = 2 \cdot S_{21}/nen \ . \tag{10}$$

Now, the absolute Z-parameter can be calculated:

$$[\mathbf{Z}] = [\mathbf{Z_{La}}]^{0.5} \cdot [\mathbf{za}] \cdot [\mathbf{Z_{La}}]^{0.5} \ . \tag{11}$$

Z_w is the complex line impedance from [8]. $[\mathbf{Z_{Lb}}]$ is the port impedance matrix with the complex line impedance.

$$[\mathbf{Z_{Lb}}] = \begin{pmatrix} Zw & 0 \\ 0 & Zw \end{pmatrix} \tag{12}$$

Using the Z-matrix, the Zw normalized Z-parameter can be calculated.

$$[\mathbf{zb}] = [\mathbf{Z_{Lb}}]^{-0.5} \cdot [\mathbf{Z}] \cdot [\mathbf{Z_{Lb}}]^{-0.5} \tag{13}$$

Finally, the renormalized S-matrix is found:

$$[\mathbf{S_{renorm}}] = [\mathbf{I}] - 2 \cdot ([\mathbf{zb}] + [\mathbf{I}])^{-1} \ . \tag{14}$$

The difference between the renormalized and the non-renormalized matching of this line is high, especially up to 20 GHz. Fig. 9 shows both reflection values of the coplanar line.

It is obvious that the source match is better at lower frequencies than higher ones. The renormalization up to 20 GHz helps achieve more realistic values.

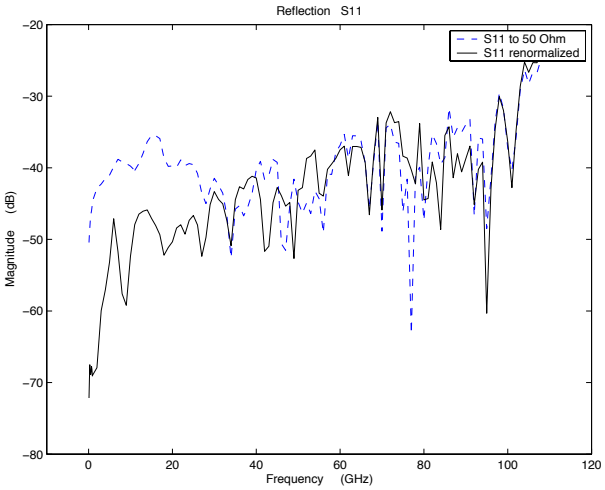

Fig. 9. Magnitude of the source match of dispersive 50 Ω coplanar line on Al_2O_3-substrate with and without renormalization

VI. Experimental Results

Based on the Numerical Simulation

At first, we calculated the S-parameter of a non-50 Ω reference line. The line impedance starts at 0.1 GHz with 60 Ω and decreases to 40 Ω at 10 GHz. The measurement error of this reference line was -65 dB up to 1 GHz and -55 dB up to 10 GHz. Fig. 10 shows both: S_{11} of this line in reference to 50 Ω and the renormalized results.

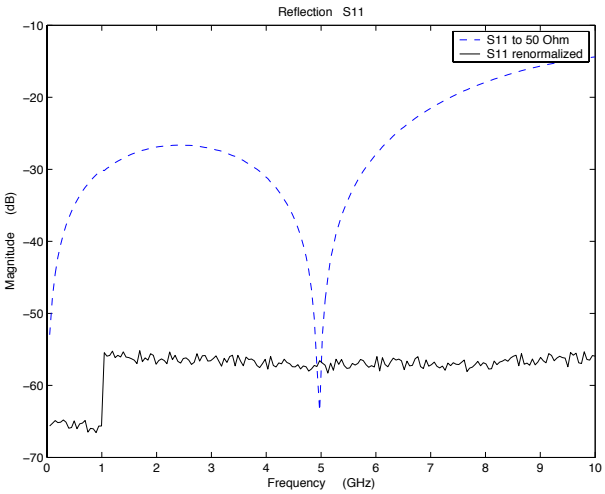

Fig. 10. Magnitude of the source match of dispersive transmission line with and without renormalization

Using this highly-dispersive reference line, the measurement error for a 55 Ω transmission line was calculated. The results in Fig. 11 show a significant decrease in the measurement error over the frequency belonging to the larger delta-match, see [2].

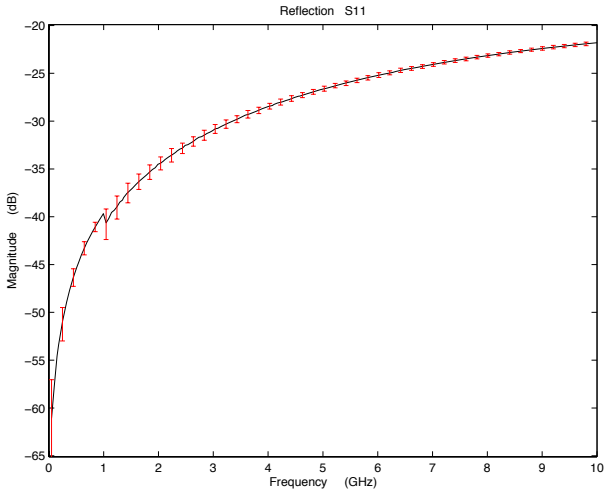

Fig. 11. Magnitude of the reflection of a 55 Ω line and calculated error bars

Based on Measurement Experiments

We used the 110 GHz PNA network analyzer from Agilent, measuring the frequency range from 0.1 GHz to 110 GHz. The calibration was performed using SussCal Professional calibration software from SUSS MicroTec and the LRM+ calibration procedure. The measurement data was exported and processed on an external computer. Additionally, the reproducibility was accepted to be -70 dB for low frequencies and -60 dB for high frequencies.

The first experimental results show the magnitude (Fig. 12) and the phase (Fig. 13) of the reflection coefficient of a 25 Ω load termination.

The final experimental results show the magnitude (Fig. 14) and the phase (Fig. 15) of the reflection coefficient of a 100 Ω load termination.

These experimental results validate the modified ripple test for on-wafer measurements. The error bars are directly generated by the source match values. Additionally, a multi-line procedure can be used to eliminate the $\lambda/2$-problem.

VII. Conclusion

This work addresses users as well as manufacturers of modern network analyzers. The theory gives worst case estimations of the reflection parameter measurement errors. Sources of measurement errors as well as the classic ripple test were explained. The background, implementation, and the on-wafer measurement results of an automatic analysis of the accuracy of S-parameter were presented. The ripple test was automated and expanded to the use of a dispersive transmission line as a reference. Numerical

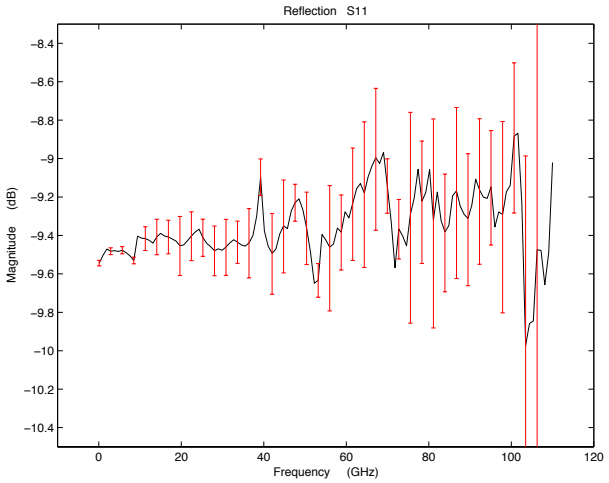

Fig. 12. Magnitude of the reflection coefficient of a 25 Ω load on Al_2O_3-substrate and calculated error bars

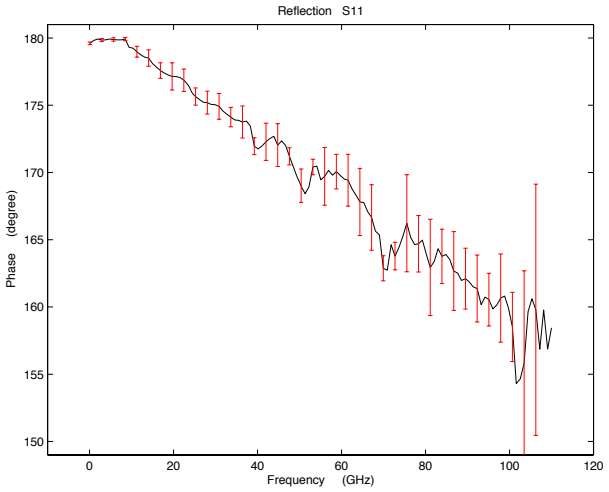

Fig. 13. Phase of the reflection coefficient of a 25 Ω load on Al_2O_3-substrate and calculated error bars

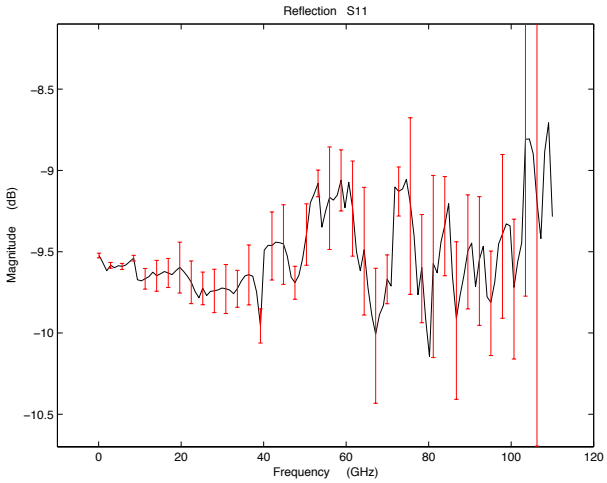

Fig. 14. Magnitude of the reflection coefficient of a 100 Ω load on Al_2O_3-substrate and calculated error bars

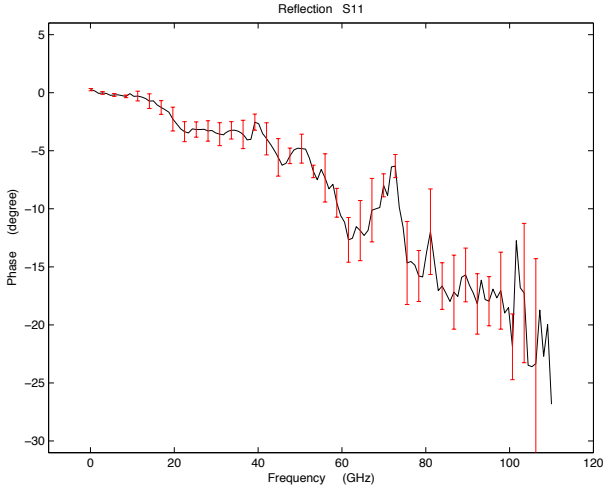

Fig. 15. Phase of the reflection coefficient of a 100 Ω load on Al_2O_3-substrate and calculated error bars

and measurement results verified the proposed automatic error bar calculation for reflection measurements.

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